



Research and Development Technical Report

SLCET-TR-85-0442-F

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MM&T FOR VHSIC MULTICHIP PACKAGES

Ron Natali  
Edwin Case

Texas Instruments Incorporated  
P.O. Box 655012  
Dallas, Texas 75265

September 1989

Final Report for Period September 1985 - September 1989

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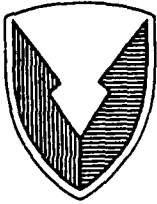
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ELECTRONICS TECHNOLOGY AND DEVICES LABORATORY

US ARMY  
LABORATORY COMMAND  
FORT MONMOUTH, NEW JERSEY 07703-5000

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<p>The objective of the LABCOM Multichip Packaging program was to develop hermetic ceramic packages suitable for interconnection of up to nine VHSIC chips operating at 100 MHz clock rates. Two packages have been designed and fabricated. One design (196 I/O) accommodated 2-4 VHSIC devices, while the other (308 I/O) accommodated 5-9 VHSIC devices. A populated 196 I/O quad SRAM module has been delivered and also five (5) each unpopulated 196 and 308 I/O packages. All electrical testing, data fixtures, methods, etc. relative to the packages and module have been delivered per Phase I contractual requirements.</p> <p>The program was divided into three phases. Phase I, originally scheduled to complete Sept. '87, was put on an accelerated schedule and completed (contd)</p>					
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19. ABSTRACT (contd)

December 31, 1986. It included design and fabrication of both package types in prototype quantities, selection of appropriate interconnect schemes, and full electrical evaluation of a populated four chip module. Also included was a survey of VHSIC community packaging requirements and development of domestic sources for package production. Phase III was scheduled to complete the project with a demonstration of limited production capability.

The total Phase I efforts represent a consolidation of responses from sixteen VHSIC contractors. The survey included factors such as package types, lead pitch, interconnects, sealing requirements, and method(s) of die attach. The packages and populated module were designed and fabricated with the survey responses taken into consideration. Through the joint effort of Texas Instruments and Interamics, Interamics was successful in delivering the needed 196 and 308 I/O packages. A VHSIC SRAM circuit was selected to prove interconnect feasibility. An alumina thick film substrate was fabricated to contain the four VHSIC SRAMS. TAB bonding was chosen as the method of die attach since single chip TAB Bonding gives the versatility of pretesting prior to mounting. Once the four chips were mounted to the substrate, the SRAM/substrate combination was electrically tested for functionality.

After sealing, the completed module was subjected to final electrical testing. This testing was witnessed by LABCOM Engineering. Due to the accelerated schedule, parallel efforts were initiated to complete packages and interconnect evaluations. These evaluations included transmission characteristics, insertion and return losses, cross talk, inductance, shunt capacitances and resistances. Power plane analysis was also performed to determine ground network resistances, maximum current capability and transient isolation. This report contains the results of the evaluation as well as package models, thermal analysis and propagation photographs.

Texas Instruments was successful in completing an environmental package evaluation, SRAM Module Analysis, CTE measurements on the packages and a package yield enhancement program, all of which are included in this report. A source for the 196 and 308 I/O packages has been established and is now available from Interamics, Inc., San Diego, CA.

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## SECTION I

### PROJECT SUMMARY/STATUS

#### 1.0 PROJECT SUMMARY

The objective of the LABCOM Multichip Packaging program was to develop hermetic ceramic packages suitable for interconnection of several VHSIC chips operating at 100 MHz clocking rates. Two package sizes were defined. One design accommodated 2-4 integrated circuits (Fig. 1), while the other housed 5-9 devices (Fig. 2). This objective was achieved by designing, fabricating, and electrically verifying both package types utilizing surveyed information from the VHSIC community and Texas Instruments (TI) advanced packaging technology.

The program consisted of three phases. Phase I was put on a six-month accelerated schedule to be completed December 31, 1986. It included design and fabrication of both package types in prototype quantities, selection of appropriate interconnection schemes, and electrical evaluation of the 2-4 chip package. Also included was a survey of VHSIC community packaging requirements and development of domestic sources for package production. Phase II would continue with the development of the 5-9 chip package and environmental evaluation. Phase III would complete the project with a demonstration of limited production capability.

The Phase I tasks were as follows:

##### TASK I - Design

- A) Conduct a survey of the VHSIC community to define the requirements for multiple chip packaging
- B) Initialize subcontractor efforts
- C) Design both package types
- D) Design a suitable interconnect
- E) Design IC mask and related tooling
- F) Design electrical test hardware and software

##### TASK II - Fabrication and Assembly

- A) Expedite subcontractor deliveries
- B) Complete IC mask fabrication
- C) Complete TAB preparation
- D) Complete electrical hardware and software fabrication

##### TASK III - Assembly and Test

- A) Assemble all stages
- B) Perform single-chip, substrate, and module tests
- C) Characterize 2-4 chip package
- D) Prepare products for delivery with final report

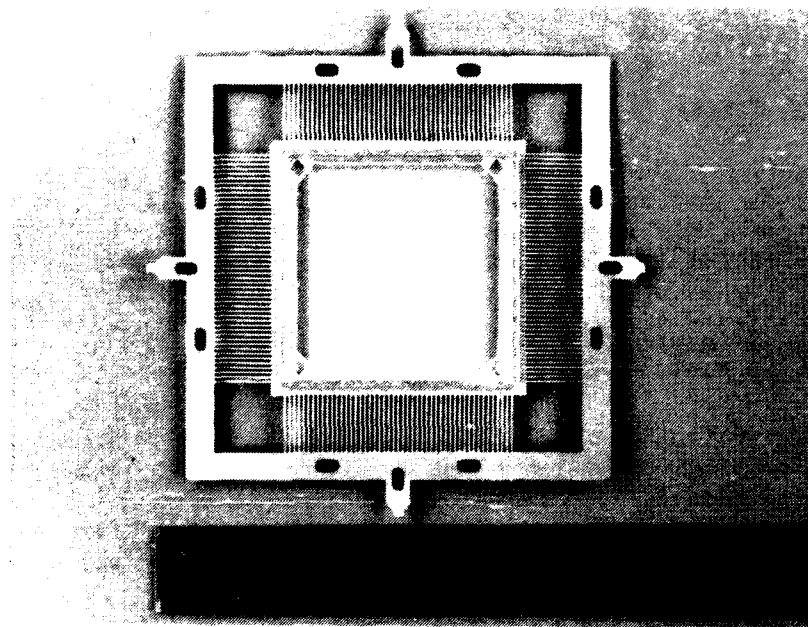


Figure 1. 2-4 Chip Package (Top View)  
196 I/O Leads - 3 Power Planes - Integral Grounding Network.

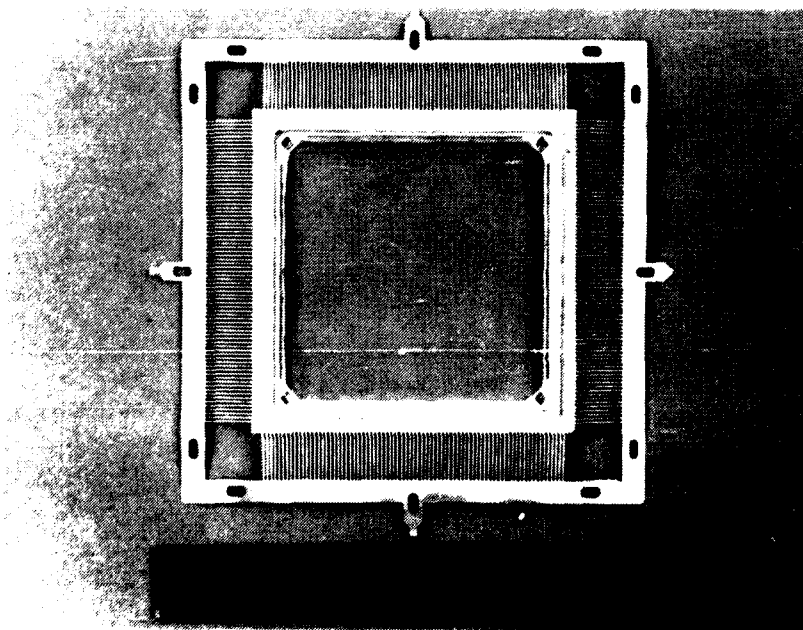


Figure 2. 5-9 Chip Package (Top View)  
308 I/O Leads - 3 Power Planes - Integral Grounding Network.

## 1.1 PROJECT STATUS

A fully functional module was delivered per contractual requirements, and submission of this data package completes the program. Figures 3 and 4 represents program schedules with applicable delivery dates. Table 1 shows delivery status of the subcontractor assemblies.

An overview of technical details is presented in the paragraphs below. Detailed test results of the SRAM circuitry evaluation and package characterization are provided in the sections that follow.

### VHSIC Survey Results

Responses received from 16 VHSIC contractors called for multichip packaging with the following characteristics:

- Leaded surface-mountable package
- Fine pitch lead spacing (.025 external, .010 internal minimum)
- Accepts a multilayer ceramic or thick-film interconnect
- Solder preform sealing with a flat Ni/Au plated Kovar lid
- Epoxy die attach with wire or TAB bonding capabilities

### Package Design

As discussed in the preliminary test plan, the packages were designed with the survey requirements in mind. The packages have the following characteristics:

- A surface-mountable leaded module
- Two package sizes: 196 I/O and 308 I/O
- The 196 lead accommodates 2-4 VHSIC devices, bypasses, and interconnect
- The 308 lead accommodates 5-9 VHSIC devices, bypasses, and interconnect
- 25 mil pitch external lead spacing
- A 1.1 inch by 1.1 inch mounting cavity for the 2-4 chip package
- A 1.65 inch by 1.65 inch mounting cavity for the 5-9 chip package
- A tungsten infiltrated copper base for improved electrical and thermal performance
- Internal ground and power planes
- Overall height of .120 inches
- Single-layer signal routing with ground plane isolation
- 'Gull wing' lead formation
- Single bond shelf with 8 mil pads on 14 mil centers
- Tungsten metallization used throughout

### Interconnect Assembly Method

- The delivered module contains a thick-film interconnect constructed by TI
- Epoxy was incorporated to adhere subassemblies as required
- Single-chip assemblies were mounted to polyimide tape and pretested
- TAB connections mated the single chips to the thick-film substrate
- The substrate was epoxied into the package and connected with 1 mil gold wire bonds

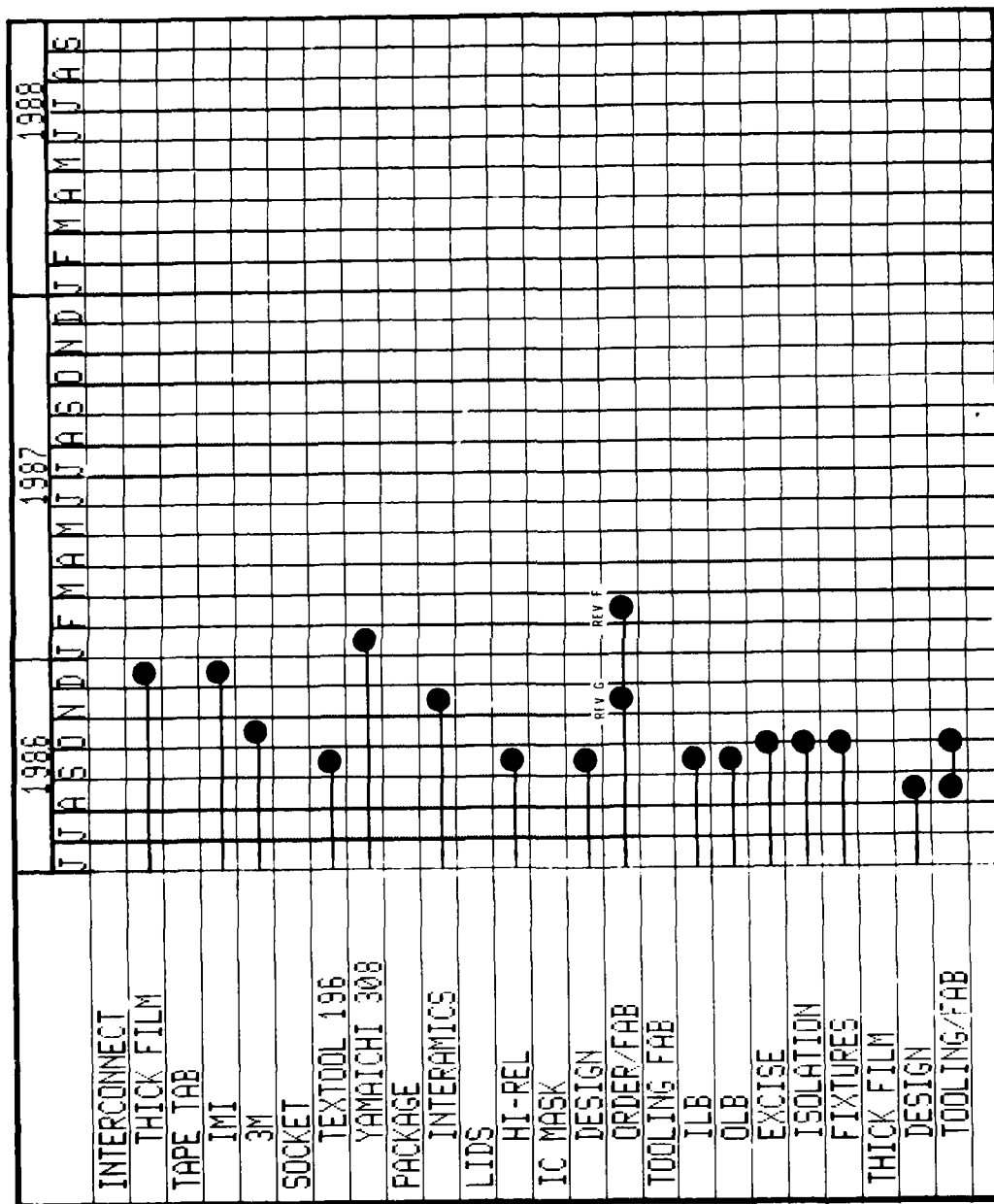


Figure 3.. Program Schedule, Prime/Subcontractor

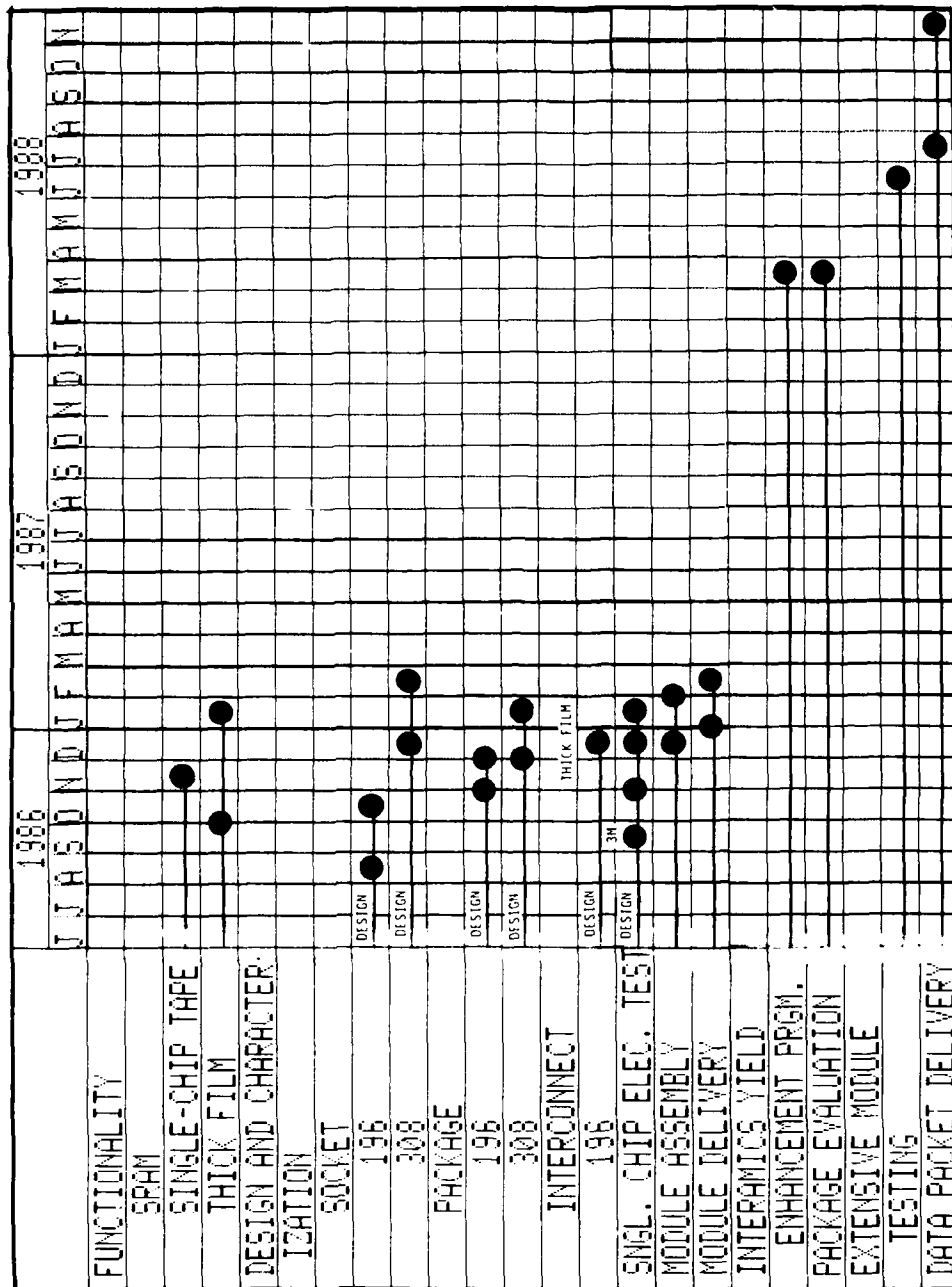


Figure 4. Program Schedule, Electrical Design/Test.

Table 1. List of Subcontractor Assemblies.

<u>Contractor</u>	<u>Assembly</u>	<u>Delivery Date</u>
INTERAMICS	196 & 308 PACKAGES	DELIVERED
IMI	35 mm SINGLE SRAM TAB TAPE	DELIVERED
3M	35 mm SINGLE SRAM TAB TAPE	DELIVERED
YAMAICHI	308 SOCKET	DELIVERED
TEXTTOOL	196 SOCKET	DELIVERED
TI	QUAD SRAM SUBSTRATE (THICK FILM)	DELIVERED
HI-REL	LIDS	DELIVERED

#### Electrical Test Approach, Functionality

- A VHSIC SRAM circuit was selected to prove interconnect feasibility
- SRAMs were tested individually at the tape level
- Four SRAMs were then assembled onto a substrate and tested (Fig. 5)
- The completed substrates were mounted in the package and tested
- After sealing, the completed module was subjected to final electrical evaluation

#### Electrical Test Approach, Characterization

- A full analysis of representative signal paths was performed with an HP8510 26.5 GHz automatic network analyzer.
- Transmission characteristics such as insertion and return loss, cross talk, inductance, shunt capacitance, and resistance were modeled and measured
- Power plane analysis was performed to include ground network resistances, maximum current delivery, and transient isolation

#### Final Reporting, Electrical

- This report contains the results obtained from the electrical characterization analysis as well as representative SRAM test data
- Additionally, package models, thermal analysis and high-speed signal propagation photographs are included.



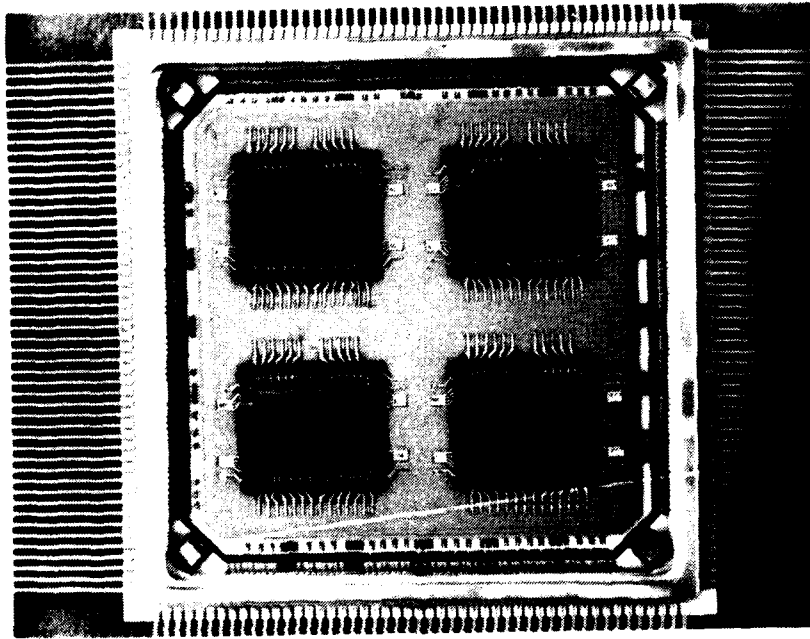


Figure 5. Completed X4 Module (Pre-Seal)  
(4) 8K x 9 VHSIC SRAMs with (4) Bypass Capacitors in LABCOM 196 Lead Package.

## SECTION II

### MECHANICAL DESIGN SUMMARY

#### 2.0 PREFACE

The following pages detail the design effort for the packages, lids, sockets, and related hardware developed for this multichip packaging program. The report begins with an analysis of the user survey which impacted the design effort. Drawings related to the mechanical design effort can be found in Appendix B.

#### 2.1 DESIGN SUMMARY

##### 2.1.1 Contractual Requirements

4.3 MULTICHIP PACKAGE The contractor shall have the option to implement either a multilayer perimeter style or pad/pin grid array (PGA) type package for this program. If a PGA package is developed, the contractor will be required to prove that reliable inspection techniques will be available. Two package sizes shall be defined: 2 to 4 chip package and 5 to 9 chip package. The number of I/Os shall be defined for typical circuit needs with the package fully populated.

4.3.1 PACKAGE SEALING Single-cavity sealing shall be utilized to the maximum practicable extent, regardless of the quantity of devices per package. Multiple seals shall be utilized only where clear advantages for this approach can be demonstrated. Package process optimized to ensure reliability of the devices during package sealing and reliability of the package seals. The package shall be hermetic in accordance with military standards.

##### 2.1.2 Introduction

The primary goal of the LABCOM VHSIC MM&T Program was to implement the technology for the design, fabrication and testing of hermetic ceramic packages suitable for interconnecting a number of VHSIC chips with a minimum loss of favorable high-speed electrical characteristics.

Because of the great diversity of VHSIC chips available and the need for a family of generic style packages which could be used to house a multitude of functional blocks, it was determined that a market survey would be the most efficient means of gathering the information needed to help set the mechanical and electrical requirements for these package designs. A survey was composed by TI engineers and disseminated to many VHSIC chip manufacturers and users to gather information on the following topics:

- Package Configuration/Style
- Dimensional Preferences - External and Internal
- Number of Bond Shelves
- I/O Pitch - External and Internal
- Drop-in Substrate Type

- Quantities and Types of Internal Passive Devices
- Power and Ground I/O Configuration
- I/O Quantity Requirements
- Power Dissipation Requirements
- Assembly Environmental Requirements
- Lid and Seal Process Preferences
- Die Attach and Wire Bonding Process Preferences
- Characteristic Impedance
- Proposed Functional Blocks and Associated Schematics

Responses were received from ten manufacturers: Allied Bendix, Boeing Electronics, General Dynamics, Harris Government Systems, Magnavox, Martin Marietta, Motorola, Raytheon, Teledyne and TRW.

### 2.1.3 Survey Responses

The primary basic package configuration selected by the responding contractors was a surface-mountable leaded chip carrier. Secondary choices were evenly divided between a leadless chip carrier style and a pin grid array. The preferred method of sealing the package was solder preform on a nickel/gold plated flat Kovar lid. A secondary selection for sealing was seam welding with a nickel/gold plated stepped Kovar lid. All users expressed the desire for thermal pads on the underside of the package.

The most preferred drop-in interconnect was a multilayer cofired ceramic substrate. A multilayer thick-film interconnect was a secondary choice. The majority of the responding users preferred an epoxy die attach and wire bonding for both chip-to-interconnect and interconnect-to-package connections though thermocompression TAB bonding was chosen as an alternative to wire bonding for the chip-to-substrate connection. Responses concerning assembly temperatures varied but the average exposure was approximately 300°C for 1 minute.

The electrical configuration responses included a few requests for a characteristic impedance of 50 or 75 ohms. A uniform response concerning dedicated contact position placed power and ground connections in each corner of the package and clocking signals entering the center of each side.

A summary of the technical information concerning the package configuration is shown in Table 2. Table 3 summarizes the information in the preceding paragraphs.

### 2.1.4 Package Design

The information gathered from the survey provided the groundwork for the package designs. The package type was dictated not only by the direct survey responses but by the requirements imposed by lead count, physical size, and desire for compatibility with high-density surface mount boards. A minimum lead count requirement of 143 pins on the 2-4 chip package and 197 pins on the 5-9 chip package along with the desired cavity sizes forced both designs beyond the limits of a reliable leadless package. This is due to the fact that leadless packages greater than approximately one inch in lateral dimension have been shown to exhibit reduced life expectancies over temperature cycling per MIL-STD-883. Therefore, a leaded package design was suggested, with leads on a minimum

Table 2. Package Characteristics

<u>Type</u>	<u>2-4 Chip</u>	<u>5-9 Chip</u>	<u>Units of Measurement</u>
DIMENSIONS:			
Outside L x W	1.5 x 1.5	2.25 x 2.25	inches
Thickness	0.100	0.100	inches
Cavity L x W	1.0 x 1.0	1.5 x 2.0	inches
Cavity Depth	0.05	0.05	inches
I/O DENSITY:			
Signal	125	175	each
Power	8	10	each
Ground	10	12	each
MINIMUM I/O PITCH:			
External	0.025	0.025	inches
Internal	0.010	0.010	inches
POWER PER CHIP:			
Minimum	0.4	0.4	watts
Maximum	3.0	3.0	watts
Average	1.5	1.5	watts
COMPONENT COUNT:			
Resistors	0	0	each
Capacitors	5	8	each
BOND SHELF:			
Quantity	1	2	each

Table 3. Package Configuration Summary

<u>Characteristic</u>	<u>Primary Configuration</u>	<u>Secondary Configuration</u>
PACKAGE TYPE:	Leaded SMT Chip Carrier	LCC/Pin Grid Array
LID:	Flat Ni/Au Kovar	Stepped Ni/Au Kovar
SEAL:	Solder Preform	Seam Welded
INTERCONNECT:	Multilayer Ceramic	Multilayer Thick Film
BONDING:	Wire Bonding	Thermocompression TAB
DIE ATTACH:	Epoxy	---
I/O PITCH:	.025 ext/.010 int	.025 ext/.010 int

of .025 pitch in order to accommodate the quantity of I/O requested by the survey respondents. An additional requirement expressed by the responding contractors was a package thickness of .100. This was relaxed to a maximum of .120 including the lid in order to correspond to JEDEC standards.

With this basic configuration defined, the next step was to determine actual dimensional requirements. An extensive study of chip sets and sizes was undertaken in order to ensure that the cavities of the two package designs were sized such that the maximum possible number of functional blocks could be accommodated. It was discovered that throughout the industry, with very few exceptions, chips are under 1 centimeter square in size (which corresponds to .394 inches). This is because most of the IC processing equipment used in the industry is configured for a maximum step size of 1 centimeter. Therefore, both packages were designed to house the maximum number of 1 centimeter chips - the small package to accommodate four chips and the large package to accommodate nine. The size of a drop-in substrate for each of these packages was determined as shown in Table 4.

Table 4. Drop-in Substrate Size Determination

<u>Small 2-4 Chip Package</u>		<u>Large 5-9 Chip Package</u>	
Clearance to substrate edge	.010	Clearance to substrate edge	.010
Bond out to package area	.040	Bond out to package area	.040
Tab or wire bonding area	.050	Tab or wire bonding area	.050
Chip	.394	Chip	.394
Tab or wire bonding area	.050	Tab or wire bonding area	.050
Clearance between chips	.010	Clearance between chips	.010
Tab or wire bonding area	.050	Tab or wire bonding area	.050
Chip	.394	Chip	.394
Tab or wire bonding area	.050	Tab or wire bonding area	.050
Bond out to package area	.040	Clearance between chips	.010
Clearance to substrate edge	.010	Tab or wire bonding area	.050
Total	1.098	Chip	.394
		Tab or wire bonding area	.050
		Bond out to package area	.040
		Clearance to substrate edge	.010
		Total	1.602

NOTE: All values are given in inches.

These figures led to nominal cavity sizes of 1.100 and 1.650 for the 2-4 chip package and the 5-9 chip package, respectively. With the cavity sizes minimized, the remaining dimensions were determined by minimizing the wire bond shelf, seal ring size, lead braze pad sizes and clearances between these features. A solder seal greater than approximately four inches in perimeter presents producibility problems. This type of seal was precluded due to the predicted sizes of the packages. A seam weld of the type used on metal packages was determined to be the most producible seal method. In consulting with VHSIC assembly engineers, the minimum allowable bond shelf width was determined to be .025 and discussions with package vendors led to a minimum lead braze pad length of .030. All of this information in addition to the JEDEC format led to the existing package outline.

The JEDEC package design format maintains an overall package dimension .150 greater than the distance between the centers of the first and last lead on each side, which is always divisible by .050. This fact along with the cavity, wire bond, and braze pad length requirements determined earlier led to the 200 lead range for the 2-4 chip package. The potential lead counts within the JEDEC format were 188, 196 and 204. With the seal ring width taken into consideration, 196 was chosen as the smallest possible lead count which would allow adequate space for all assembly processes. In addition, a lead count of 196 was already being introduced into the industry by other companies and 3M/Textool had already tooled a socket for this package outline (see Socket Design section). The package OD is 1.250 square. A mechanical drawing of the 196-lead package can be found in Appendix B as TI drawing #2795724.

The 5-9 chip package was sized in a similar manner although additional seal ring width and bond shelf width were allocated due to the larger overall dimensions and, thus, tolerances. A lead count of 308 was chosen for the larger package yielding an OD of 2.050 square. A mechanical drawing of the 308-lead package can be found in Appendix B as TI drawing #2795722.

General specifications for both of the packages can be found in Appendix B as TI Specification Control Drawing #2795713.

With the basic physical dimensions of both packages set, the detailed design of the packages began to evolve. Many basic concerns immediately became evident due to the sheer physical size of the packages. Tolerances on lateral dimensions, layer-to-layer alignment and cavity and seal ring flatness were critical issues requiring careful attention. The desire by the survey respondents, as well as TI VHSIC engineers, to introduce bypass capacitors internal to the package was also a major concern. All of these issues were addressed in order of their impact on package design.

The most likely mode for chip-to-chip interconnect was found through the survey to be some type of drop-in substrate - whether thick-film, thin-film or an organic multilayer circuit. Although direct deposition of thin-film or other organic multilayer interconnects onto the package base may be a preferred technology in the future, this technology was still under development and not yet standard in the industry. So the decision was made to design the package primarily to be very generic in accommodating virtually any type of conventional drop-in substrate. Prior to the commitment to drop-in substrate compatibility, a wholly ceramic package design was proposed with buried power and ground planes spanning the entire package base. These planes could be accessed through a matrix of vias exposed on the cavity surface. This design concept would have been practical and effective for a directly deposited multilayer interconnect. However, it would be of little use with a drop-in substrate since any connection from the chip to the buried power or ground planes would have to be routed through the substrate multilayer interconnect and to the package bond shelf before reaching the buried planes. There are also severe flatness problems with cofired packages involving large cavities (over 0.5 inches square). This flatness or camber concern combined with thermal issues led to the use of a thermally and electrically conductive tungsten/copper base having a thermal expansion coefficient that closely matches that of the alumina ceramic package

material. This type of package base virtually eliminates any camber problem, provides an excellent thermal spreading effect, and in fact, behaves as a thermal short when soldered or otherwise directly mounted to the board or thermal plane.

At this point, the final package configuration had evolved into cofired multilayer alumina 'windowframe' brazed onto a tungsten copper base plate with a Kovar seal ring and a Kovar lead frame brazed onto the top of the ceramic 'windowframe.' This basic configuration was reviewed and refined by both TI and Interamics personnel.

Extensive electrical modeling and analysis led to an electrical design that includes three dedicated power 'rings' - one for each of the three voltages typically used on VHSIC chips. Above these three ring-planes are two ground planes with the signal/power/ground trace layer sandwiched between, effecting a microstrip configuration. The use of a single bond shelf allows assembly of the substrate into the package using either TAB or conventional wire bonding techniques. Analysis prescribed the use of multiple dispersed power and ground I/O connections, rather than the single-point grounding scheme used in previous package designs, resulting in a total of 20 power and ground I/Os for the 196 lead package - 2 ground leads per side and one each of the three power leads per side. The 308 lead package contains 28 power and ground I/Os - 3 grounds per side, two primary power leads per side and one each of the remaining two power leads per side. This arrangement of leads allows equal access to all ground and voltage from any quadrant of the drop-in substrate which, in turn, facilitates routing of the drop-in multilayer and minimizes IR drop and signal lead length in the interconnect. The seal ring and base are also tied to ground. The layup of the metalization layers is shown in Table 5.

Table 5. Layup of Metalization Layers

Metal Layer 7	Braze pads for seal ring and lead frame (Ground)
Metal Layer 6	Ground
Metal Layer 5	Signal/Power/Ground trace layer
Metal Layer 4	Ground
Metal Layer 3	Primary Power
Metal Layer 2	Secondary Power
Metal Layer 1	Tertiary Power
Metal Layer 0	Braze area for tungsten/copper base (Ground)

After the basic configuration, layup, and footprint were defined only the final dimensioning in the z direction and the incorporation of capacitors into the package remained unfinished. The combination of package external height or thickness restrictions, large z-axis tolerances on cofired ceramic, and the introduction of chip capacitors into the package presented great difficulties. An overall thickness of .120 for a sealed package was the goal, with the internal cavity height maximized in order to accommodate the largest possible capacitor. Extensive negotiation between TI and Interamics engineers was involved in determining the effect of tolerances on the assembly of these parts.

With respect to capacitor location, the design lent itself to placement of a single capacitor in each of the four corners of the package. This allocated two capacitors for the voltage which would experience the highest switching current, and one capacitor each for the remaining two voltages. An R11 capacitor size was targeted, allowing a value of up to .047 microfarads to be obtained. Cavities were designed in each of the corners to house the capacitors. This resulted in only a minor change in the substrate cavity sizes. Substrate cavities in both the 196 lead and 308 lead packages had to be modified to incorporate a .102 x 45° chamfer at each of the four corners to allow the R11 capacitors to fit, but this had no real effect on the substrate's capacity to accommodate the VHSIC chips since the corners would be virtually unused anyway.

The dimensions of several of the components of the package assembly were determined by mechanical or process constraints. A thickness of .020 was determined to be the minimum for the package base to maintain structural stability. The base thickness dimension has a tolerance of .002. The flange on the stepped lid was set by sealing process parameters at .005 with a negligible tolerance. Welding process guidelines also fixed the seal ring thickness at .040 nominal to prevent any braze reflow from occurring. A 10% tolerance on the cofired ceramic layers was taken into consideration and the remaining requirement was a minimum internal height above the capacitor mounting area of .055 which included a maximum R11 capacitor height of .040, allowance for epoxy mount, and clearance to the lid.

Based on all the restrictions and requirements detailed above, the final design was formulated. Seven ceramic layers were required for the eight metalization layers listed in Table 5. In order to accommodate the internal bypass capacitors and still fall within the .120 JEDEC height ceiling, a thickness of .007 nominal was indicated for the ceramic layers. The capacitor mounting pads were placed on top of the second ceramic layer instead of the first to ensure structural stability of the windowframe. The z-axis stackup in the capacitor mounting areas is shown in Table 6.

Table 6. Stackup for Capacitor Mount

<u>Component</u>	<u>Nominal (inches)</u>	<u>Minimum (inches)</u>
Layers 3 through 7	.035	.0325
Seal Ring	.040	.036
Lid	-.010	-.011
Total	.065	.0575

The resulting z-axis overall package layup along with minimum and maximum dimensions is shown in Table 7. For assemblies in which all components are concurrently at worst case thicknesses, the package would be outside the height ceiling of .120. It is unlikely that this would occur, especially since the 10% tolerance on the cofired ceramic multilayer windowframe is an absolute maximum which is not normally experienced. All cofired ceramic manufacturers are working toward improving this thickness tolerance and it should continue to



decrease in the future. If, in fact, the assembly does stack up to a thickness above the height ceiling (greater than .115 for an unsealed package), the vendor will be required to grind the seal ring in order to bring the assembly under the height ceiling.

Table 7. Package Z-axis Layup

<u>Component</u>	<u>Nominal (inches)</u>	<u>Minimum (inches)</u>	<u>Maximum (inches)</u>
Base	.020	.018	.022
Layers 1 and 2	.014	.0126	.0154
Layers 3 through 7	.035	.0325	.0385
Seal Ring	.040	.036	.044
Lid	<u>.005</u>	<u>.005</u>	<u>.005</u>
Total Package	.114	.1041	.1249 (See Text)
Total Substrate Cavity Depth	.084	.0741	.0949
Total Capacitor Cavity Depth	.065	.0575	---

In summary, the package designs are generic and can be used to house almost any set of VHSIC chips. The multipoint power and ground scheme is appropriate for use at VHSIC speeds and the I/O count of both packages is sufficient for almost any particular functional block. The package configuration is thermally efficient and the electrical characteristics are desirable (see electrical section of this report).

#### 2.1.5 Lid Design

The two lid designs were basically dictated by process parameters for seam welding. Based on the seal ring sizes, which were determined from the overall package sizes, the lids were designed to be a total of .005 smaller than the outside dimension of the seal ring. A Kovar lid with electrolytic gold over electrolytic nickel plating was specified since this material combination matches that of the seal ring. A .005 thick flange was specified with a flange width of .050. An overall lid thickness of .015 was specified. This thickness provides structural stability on both packages as long as leak testing per MIL-STD-883 was done at the low end of the pressure scale. A thicker lid could be introduced, especially for the 308 lead package, if the thickness would not interfere with the circuitry and parts on the drop-in substrate. To allow for the capacitors, the lid could be etched out in the capacitor mounting areas just as it is in the flange area to provide an increased height ceiling in those areas. A drawing of these lid designs can be found in Appendix B as dash numbers -7 and -8 in TI Source Control Drawing #2891091.

After both package types were received and reviewed, it was found that the seal ring experienced a small degree of bowing toward the center of each of the four sides which caused the lid to be slightly oversized at these points. Since it is important for the lid to be only a few mils within the seal ring in order to achieve successful seam welds, the lid designs were modified to be .005 smaller than the original designs. This is, in essence, a total of .010 smaller than the nominal seal ring dimension. A drawing of these latest lid designs can be found in Appendix B as dash numbers -13 and -14 in TI Source Control Drawing #2891091.

#### 2.1.6 Socket and Extraction Tool Design

The design and procurement of test sockets for both the 196 lead and the 308 lead packages were important parts of the program since electrical testing and characterization really cannot be done without them. In the case of leaded packages, especially fine pitch ones which can be quite fragile, the design of a carrier to protect the package during assembly and test is also critical. For the LABCOM VHSIC Multichip Package Development Program, the carrier and socket were designed so that the all-purpose carrier was compatible with the socket and the part could be inserted into the test socket without being removed from the carrier. This minimizes the packages' exposure to potential damage. As previously mentioned in this section, a socket/carrier combination for the 196 lead package had already been tooled by 3M/Textool for use by LSI Industries. This set was purchased for use with the 196 lead package. A package loading and extraction tool was required for use with the Textool carrier. This tooling was designed and built by TI and a drawing of the tool can be found in Appendix B under the title "Loading Fixture for the 196 Lead Package Carrier."

Unlike the 196 lead socket and carrier, the 308 lead package required new custom tooling for its socket and carrier. An appraisal of potential suppliers yielded a range of quality and price so samples from each of these suppliers were obtained and evaluated by TI test engineers for performance, reliability, and overall suitability for this application. There were only three vendors capable of building a socket of this type and Nepenthe/Yamaichi by far outdistanced the other two in virtually every area. The Nepenthe socket is a high-quality, dependable part. All contact pins are positioned securely in the socket base, unlike those of their competitors. The carrier uses a latching mechanism and, thus, requires no loading/unloading fixturing. Location of the carrier with respect to the socket base is accomplished through the use of precisely located steel pins, ensuring consistent contact between package and socket. Additionally, TI was already using the 172 pin version of this socket successfully on another program. Drawings of the 308 lead socket and carrier were purchased from Nepenthe and drawings of them can be found in Appendix B under the titles "Socket, LABCOM 308 Lead" and "Carrier, LABCOM 308 Lead."

#### 2.1.7 Lead Form and Clip Tool Design

A lead forming and clipping tool was needed for both of the packages. A lead formation for surface mounting the packages was defined and is shown on TI drawings #2795722 and #2795724 in Appendix B. Based on this lead formation an existing generic forming and clipping tool design was modified to accept both the 196 lead and 308 lead packages. This is a spring-loaded fixture that performs all actions including clamping, forming, and clipping of the leads. A drawing of the tool can be found in Appendix B as TI drawing #M-A-2686134.

## SECTION III

### PROCESS SUMMARY

#### 3.0 INTRODUCTION

The following pages contain a detailed discussion of the steps involved in the assembly of the module from fabrication of the thick-film interconnect to final sealing. The information is presented in a format that follows the Assembly Work Orders found in Appendix A for each of the assembly levels. Each step in the construction process is identified and detailed. A set of photographs of the equipment used can be found in Appendix D. Detailed artwork for the thick-film interconnect is provided in Appendix E.

#### 3.1 CONTRACTUAL REQUIREMENTS

4.3.10 CHIP INTERCONNECTION The contractor shall specify the type of interconnection system that will be used; e.g., multilayer ceramic, TAB, area TAB, etc. The method selected shall stress low capacitance, resistance, and inductance. The interconnection method must be flexible such that customized signal layers can be incorporated into the package design. If a polymer is used, the amount of this material shall be minimized to reduce possibility of moisture in the package. The chip interconnection definition shall be accomplished using CAD routing.

#### 3.2 THICK-FILM INTERCONNECT DESIGN

##### 3.2.1 Circuit Definition

Purpose - To clearly define all requirements of the finished part before any layout work begins.

Procedure - Obtain a finalized version of a detailed schematic and do any required worst case analysis to determine any potential problems with high current paths or signal lines susceptible to cross talk or noise.

##### 3.2.2 Recognition of Special Limitations

Purpose - Recognize any special situations unique to the project at hand and define any compromises needed to accommodate those situations.

Procedure - Define the special requirements and how the normal flow will need to be altered to accommodate those requirements. In the case of the VHSIC interconnect, special requirements included such items as a predefined substrate shape and size, predefined I/O pad locations, the need for extra ground planes as shields, and the preference for having no top-layer interconnections to enhance both aesthetics and yield in the TAB bonding process.

### 3.2.3 Artwork Generation

Purpose - Generate physical patterns on a scale large enough to maintain necessary tolerances.

Procedure - Cut-and-peel rubylith artwork is generated and meticulously checked for continuity and adherence to design inputs.

### 3.2.4 Film Reduction

Purpose - Reduce the rubylith artwork to 1X for use as photomasks.

Procedure - The artwork is photographically reduced in one or multiple steps and printed on high-definition film.

## 3.3 THICK-FILM INTERCONNECT FABRICATION

### 3.3.1 Screen Fabrication

Purpose - To generate screens for use in screen printing.

Procedure - Expose the photosensitive emulsion on the screens through the photomasks thus transferring each layer pattern to a screen.

### 3.3.2 Screen Print

Purpose - To physically print the layer patterns onto a substrate.

Procedure - Alternate layers of conductor and dielectric are printed on the ceramic substrate by forcing appropriate inks and pastes through the patterns on the screens in a screen printer. Each layer is dried for a short period and then fired in a belt furnace to purify and stabilize the material into its final state. Seven dielectric and eight conductor layers were alternately printed and fired for this particular part. All screen printing was accomplished with an AMI Presco #885 screen printer. Drying and firing was done in a BTU #DR854D drier and a BTU #TFM 82230B460N48 furnace.

### 3.3.3 Laser Scribe and Break

Purpose - To remove from the substrate excess ceramic necessary during screen printing but not acceptable on the finished part.

Procedure - A laser is used to cut partway through the substrate along the final dimension lines and then all excess ceramic is broken away from the part along those scribe lines. Scribing uses a low-power laser beam to avoid much of the splattering that occurs when drilling completely through the substrate. Some laser drilling prior to screen print was also done on these parts to accommodate the chamfered corners. All laser scribing and drilling was done with a Coherent General #M46 CO<sub>2</sub> laser.

### 3.4 TAB TAPE ASSEMBLY

#### 3.4.1 Wafer Inspection

Purpose - To inspect the wafers prior to metallization with TiW and gold.

Procedure - Each wafer must be inspected for contamination by oil, dust, dirt, fibers, or other residues. If contamination is found, indicate the problem on the trouble sheet and clean the wafer. Reinspect after cleaning. If the contamination is still present, contact process engineer. The wafer shall also be free of any scratches greater than .250 inches. If scratches do exist, record them on the trouble sheet. The pads of the individual die must also be inspected to ensure that they are free from damage from probing and residual protective oxide. Record any discrepancies.

#### 3.4.2 Metallization

Purpose - An adhesive, barrier, and protective layer of metallization must be deposited on the wafer to provide a seal for the aluminum bond pad. The metallization must also provide a current conducting path for plating of the gold bump.

Procedure - A TiW alloy/gold metallization system was chosen. The Ti/W provides excellent adhesion to the aluminum bond pad, as well as providing a barrier to the gold. The gold serves as a protective layer to the Ti/W and also is capable of carrying the plating current. This metallization is DC magnetron sputtered in an MRC 903 system (Appendix D, Fig. D-1). The thickness of the Ti/W is 1500Å and the gold 5000Å. The thicknesses are checked using a Veeco Series 5000 four-point probe (Appendix D, Fig. D-2).

#### 3.4.3 Photoresist

Purpose - A method to mask off all but the I/O or bond pads of each chip is required to provide a plating mask for the gold bumps.

Procedure - The wafers are photoresisted using a Zicon series 10,000 auto-coater (Appendix D, Fig. D-3). American Hoechst Corporation's AZ-4902 photoresist is used to coat the wafers. The photoresist is deposited in a three-step process with soft bakes in between each spray, until a final thickness of 22-25 microns is obtained. The wafers are soft-baked in a Blue M forced air oven to drive out any remaining solvents (Appendix D, Fig. D-4). Two blank wafers are always run with the live SRAM wafers for exposure and thickness measurements. The thickness checks are taken using a Tencor Alpha Step 200 profilometer (Appendix D, Fig. D-2).

#### 3.4.4 Exposure and Development

Purpose - In order to plate the bond pads of the chip, exposure and development out of the pads is required to create a window in which to plate.

Procedure - The wafers with the photoresist in the soft-baked condition, are loaded into a Canon PLA 501F proximity printer (Appendix D, Fig. D-4). The mask used to expose the wafers is a modified protective overcoat mask. The mask is manufactured from quartz with an antireflective chrome surface. The only openings on the mask are that of the bond pad pattern. The bond pad openings are reduced in size to allow for photoresist flow during hard bake. One blank wafer is aligned to the mask and exposed in the hard contact print mode of the Canon. This wafer is then developed in AZ-421K developer for a fixed period. The wafer is then inspected under an infrared scope (Appendix D, Fig. D-5) to ensure that there is no residual photoresist on the bond pad. Photoresist will fluoresce under infrared light. If there is residual photoresist then the exposure time is increased and another blank wafer is run through the sequence. When the final exposure time is determined for this batch of wafers, then the live SRAMs are processed. Following the correct exposure and development of the resist, the wafers receive a final hard bake to drive out all of the remaining solvents.

#### 3.4.5 Inspection of the Photoresist

Purpose - To ensure that the bond pads are clear of any residual photoresist contamination, and to repair any defects that are present in the resist.

Procedure - The wafers are once again examined under the infrared scope to check for resist in the area to be plated. If any is found, then the wafers are stripped and reprocessed. Any "dinks" or imperfections in the photoresist are manually repaired by painting over the open areas with some photoresist in order to cover up these spots so that they will not plate.

#### 3.4.6 Gold Bump Plating

Purpose - Tape automated bonding requires some type of bump to which to bond the TAB tape. The bumps used for the VHSIC SRAMs are electroplated gold bumps. This gold bump, together with the metallization, also provides a seal for the easily corroded aluminum bond pad. These bumps should be in the 90 knoop hardness range in order to provide cushioning to the bond pad during bonding.

Procedure - An IMI EPM 149-2 bump plater is used (Appendix D, Fig. D-5). This plater is referred to as a fountain-type plater due to the inverted manner in which the wafer is presented and the water bubbler type arrangement of the plating solution flow. There are three cathodic connections to the wafer via teflon-coated pins and a platinized titanium anode which is directly opposing the slice. The plating bath is Selrex 309 solution, which is plated at a current density of  $4 \text{ A/ft}^2$  for 80-100 minutes. The resulting bump height is 22-25 microns.

#### 3.4.7 Photoresist Strip

Purpose - It is necessary to remove the photoresist to enable the eventual removal of the TiW/Au metallization covering the wafer and shorting all the chips together.

Procedure - The AZ-4902 is easily removed by rinsing in acetone.

#### 3.4.8 Gold Etching

Purpose - To remove the thin-film sputtered gold layer.

Procedure - The wafers are first ashed in a Microscience Plasmalab plasma reactor (Appendix D, Fig. D-6) at 100W for 3 minutes. This is to ensure a clean surface prior to the wet gold etch. This is imperative in order to achieve a uniform etch rate over the entire wafer. The wafers are etched using a wet cyanide etch. Each wafer is done individually in beaker format. The trade name for the etch is Technistrip II. Following the gold etch the wafer receives a thorough rinsing in DI water.

#### 3.4.9 Ti/W Etching

Purpose - To remove the thin-film sputtered Ti/W layer.

Procedure - The wafers are once again processed a single wafer at a time in a beaker. Ti/W is etched using a heated solution of 30% hydrogen peroxide. A few grains of ferrous ammonium sulfate are added to reduce the possibility of Ti/W residues. When the Ti/W is removed, the wafer is rinsed in DI water for at least 5 minutes to ensure that all of the etchant is diluted and the wafer is clean.

#### 3.4.10 Wafer Mounting

Purpose - The wafer has undergone a series of process steps, all of which have resulted in there now being a gold bump where before there was just an aluminum bonding pad. The wafer mounting step prepares the wafer to be sawed into individual chips.

Procedure - The wafers are mounted on a sticky tape and this tape is stretched onto a metal frame which is held in the saw. This allows the chips to be sawed all the way through. This eliminates the usual edge burr problem associated with breaking the chips should one use the scribe-and-break routine. Edge chipping and corner cracking are virtually eliminated.

#### 3.4.11 Wafer Dicing

Purpose - To separate the wafer into individual chips.

Procedure - The wafers are diced on a Microautomation dicing saw (Appendix D, Fig. D-7). There were no unusual processes or procedures required, and sawing was completed in accordance with standard sawing techniques.

#### 3.4.12 Inspection of Diced Chips

Purpose - To inspect individual chips after dicing for defects that will make the chip unbondable or nonfunctional.



Procedure - Inspect every bump on a chip to ensure that it is correctly formed and that:

- There are no large nodules on the bump.
- The bump is centered in the aluminum.
- There are no scratches on the chips or bumps.
- The bumps are not shorted.
- There is no excess gold or other contamination on the chips.

If scratches, voids, discoloration, corrosion, bridging, or any other defect of the metallization or bumps is noticed, then the chip will be rejected.

#### 3.4.13 Interlead Bonding

Purpose - The chips with 22-25 micron high gold bumps are now assembled to 35 mm TAB tape. Two different tape designs were used. The first tape was designed to be mounted in the cavity of an interconnect, appropriately the TAB leads had a bend or a kink in them to act as a stress relief. This tape was manufactured by 3M Corporation and is a two-layer tape. The delivery of the interconnects for which this tape was designed was questionable. Therefore, a second tape design was initiated. This tape design has straight leads and is designed to withstand a mechanical lead-forming operation. This tape is a three-layer construction and was laminated by International Micro Industries (IMI) and etched by Mesa Corporation. The latter tape was used for interconnecting the chips to the TI multilayer thick-film substrate.

Procedure - Innerlead bonding is accomplished on an IMI 1207 bonder (Appendix D, Fig. D-8). This bonder is a manual laboratory type. The TAB tape is gold plated and the bumps on the chip are also gold, a gold-to-gold thermo-compression bond is therefore created. The chips and the tape are presented in a singular manner, are positioned to each other with a mechanical joystick and bonded using a flat solid heated tool. The chips are also back-headed to decrease the thermal shock of the bonding tool.

#### 3.4.14 Innerlead Bond Inspection

Purpose - To ensure that all of the TAB leads are bonded and aligned.

Procedure - The TAB-bonded chips are first checked for alignment. The leads should not extend more than 50% across the space between the pads. A visual check of the bonding of the leads is then done. The innerlead bonding tool will leave a bright mark on the leads. Any lead not marked or otherwise appearing unbonded is checked on the Dage Microtester 22 (Appendix D, Fig. D-9). The leads must withstand a nondestructive test of 10g.

#### 3.4.15 Isolation Tape

Purpose - The leads on the TAB tape are all electrically shorted together. The tape is manufactured in this manner to enable the electroplating of gold. In addition, this provides increased static protection for the chip during innerlead bonding. These leads must therefore be separated from each other in order for the chip to be electrically tested on tape.

Procedure - A punching die to perforate the gold-plated copper busing bars for the IMI single chip TAB tape was manufactured (Appendix D, Fig. D-10). This punch was not successful in isolating all of the leads due to some minor design errors in the TAB tape. It was necessary to further cut the TAB tape with an X-acto knife. This problem is easily solvable through proper TAB tape design and is of no concern. Since the leads are all separate, the chip is easily static damaged so ground straps and air ionizers should be used.

#### 3.4.16 Electrical Test (See Electrical Section for Details)

#### 3.4.17 Excise

Purpose - The leads of the single-chip TAB must be cut to the proper length to allow for its mounting to the interconnect.

Procedure - A punching die was fabricated (Appendix D, Fig. D-10) to shear all of the leads at once to the correct length. The single-chip TAB is loaded individually into the die set, then the level press is lowered and the finished part is removed. Once again static protection techniques should be utilized.

#### 3.4.18 Die Mount

Purpose - The die must be mounted to provide a thermal and mechanical link to the interconnect. For LABCOM the interconnect is a thick-film ceramic multilayer board.

Procedure - The dies are lead-formed using a forming tool (Appendix D, Fig. D-10). Once the leads are formed, a small amount of Amicon C-990 epoxy is dispensed in four places onto the interconnect. The chips are then manually mounted onto the interconnect and positioned properly. The epoxy is then cured in a vacuum oven.

#### 3.4.19 Outerlead Bonding

Purpose - To electrically and mechanically connect the single-chip TAB parts to the interconnect.

Procedure - The VHSIC SRAMs were outer-lead bonded on a TI modified K and S single-point manual thermosonic wire bonder. The four-chip substrate is loaded into the bonder on a heated stage. The bonding tool is also heated and is an ultrasonic horn. The tool is brought in contact with the TAB tape and the ultrasonic power is applied. The metallurgy of the bond is a gold TAB tape to the gold thick-film. The wide power and ground TAB leads were bonded twice to provide a good electrical connection area.

#### 3.4.20 Outerlead Bond Inspection

Purpose - To visually inspect the outerlead bonds for shorts or opens, as well as any other defects.

Procedure - The four-chip module is bonded to the thick-film substrate. At this point, a thorough visual inspection is done to check the chip, TAB, and substrate for defects. Defects include scratches, debris, bent leads, unbonded leads (both inner and outer), and cracks.

### 3.5 MODULE ASSEMBLY

#### 3.5.1 Substrate Mount

Substrate attachment was performed with Ablefilm ECF-550-1 conductive epoxy film which was cured at 170 +/- 10°C for 1.0 +/- 0.1 hours in a temperature monitored oven.

#### 3.5.2 Wire Bonding

Package interconnect was accomplished with a Mech-E1 Model 827 thermo-sonic ball bonder. One mil gold wire of 99.975% purity was used as the interconnect material.

#### 3.5.3 Wire Bond Inspection

All wire bonds were inspected at 30X magnification for current placement and visual criteria requirements per MIL-STD-883C, Method 2017.

#### 3.5.4 Bond Strength

A 2g nondestructive bond strength test was performed on 100% of the bonds with a Dage MCT20 microtester per MIL-STD-883C, Method 2023.

#### 3.5.5 Preseal Electrical Test

An electrical test was performed in accordance with the procedures outlined under functional testing in Section II of this document.

#### 3.5.6 Package Seal

Package sealing was performed in a dry nitrogen atmosphere with less than 10 PPM water vapor on a Model 161 Superior Lee Seam Welder.

#### 3.5.7 Visual Mechanical

Prior to final electrical test, a visual mechanical inspection was performed to ensure conformance to MIL-STD-883, Method 2009.7.

#### 3.5.8 Final Electrical

A final electrical test was performed in accordance with the procedures outlined under function testing in Section II of this document.

## SECTION IV

### TEST RESULTS

#### 4.0 INTRODUCTION

Electrical testing was partitioned into two separate tasks. The first task undertook to provide pretesting capabilities and interconnect verification. The second task was designed to verify the electrical performance of the package at digital clocking rates of 100 MHz. The first task was termed 'Functional Testing' and the second task was termed 'Characterization Testing.' Tables 8 and 9 summarize the efforts completed for each task.

Table 8. Functionality Testing Subtasks.

<u>Task</u>	<u>Performed On</u>
Wafer probe	SRAM slice
TAB tape test	Single SRAM mounted to 35mm tape
Substrate test	Quad SRAM on interconnect
Module test	Quad SRAM interconnect mounted in package
Final test	Quad SRAM in sealed 196 lead package

Table 9. Characterization Testing Subtasks.

<u>Task</u>	<u>Performed On</u>
Continuity test	All conductors - 196 & 308 lead packages
Transmission characteristics	Signal lines - 196 & 308 lead packages
Power plane analysis	3 power planes - 196 lead package only
Current delivery	Power/ground networks - 196 lead package
Grounding network analysis	Ground network - 196 lead package

#### 4.1 CONTRACTUAL REQUIREMENTS

4.3.9 ELECTRICAL PROPERTIES Critical electrical parameters of the package, with respect to VHSIC device and system performance, shall be optimized to the maximum extent feasible. Package trace resistance, capacitance, and inductance, along with ground plane resistance and proximity to signal lines, shall be appropriate to meet VHSIC chip applications with system clock rates of 100 MHz.

4.3.11 CHIP PRETESTABILITY A suitable approach shall be chosen to permit the pretesting of VHSIC chips before they are mounted into a package.

#### 5.2 TEST PLAN Special provisions

- a. Electrical characterization of packages including R, L, and C measurements of I/O lead metallization and package insulation resistance.

- b. Electrical characterization of chip interconnect system using VHSIC or VHSIC-like chips.

#### 4.2 SUMMARY OF TEST SEQUENCE

Package and interconnect integrity was verified by electrically testing four VHSIC SRAMs using the equipment shown in Figs. 6 and 7. Testing was performed at 25°C using the standard final test program for the individual SRAM's. Chip select lines were engaged to test each of the four SRAM's individually.

Each SRAM was probed on TAB tape for full operational parameters. Once mounted to the substrate, the entire assembly was probed again. The final two tests were executed with the substrate mounted into the package and then with the package sealed. The following pages provide the details of the functional testing sequence.

#### 4.3 EXPLANATION OF SENTRY 21 SRAM TEST RESULTS

##### 4.3.1 Introduction

The following is an explanation of the test data log printout produced by the Fairchild Sentry 21 tester during the test of a TI 8K x 9 VHSIC SRAM. Included is an actual data log from the Sentry that was produced during SRAM testing for the LABCOM VMC program. The printout has been broken up to better facilitate the explanation. Also included are some example printouts that illustrate the different data logs produced by the Sentry for each of several different test results. These examples include both successful and unsuccessful test data logs.

##### 4.3.2 Header

The header simply contains date, time, and serial number data and identifies the program being executed.

(Station 3)	(Date)	(Time)	
STAT3	01-20-87	09:03	
TEST PROGRAM	TSRAM	S/N	11
(Program Identification)		(Device Serial Number)	



Figure 6. Sentry test system with SRAM probe station.

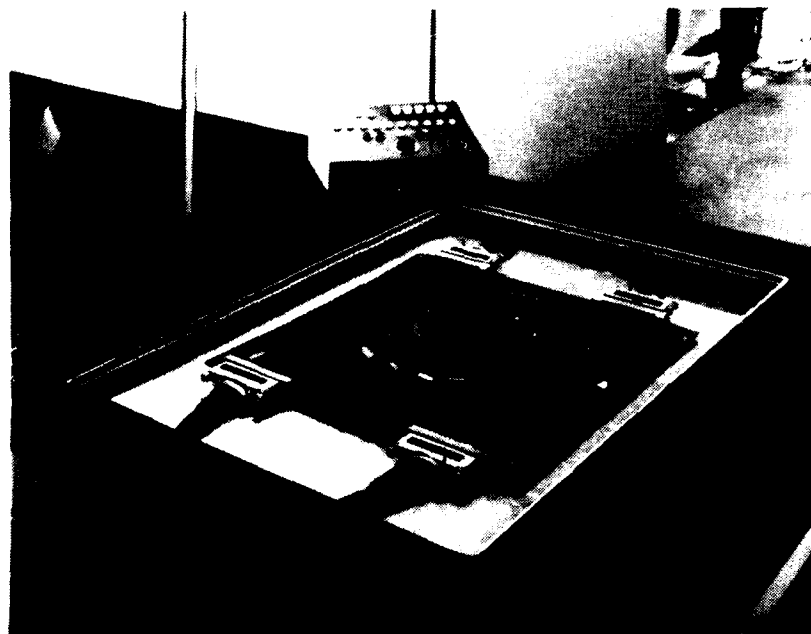


Figure 7. Sentry test head with 196-lead socket.

#### 4.3.3 Address Byte Pair Search

This part of the test steps through the address pairs of the SRAM and measures the chip select access times. The access times printed should be multiplied by 10E-10 seconds.

(26 Address Pairs)				(Chip Select Access Times - Non Pipe)										
(Add sw)	(Row Col)	(Row Col)		(DQ0)	(DQ1)	(DQ2)	(DQ3)	(DQ4)	(DQ5)	(DQ6)	(DQ7)	(DQ8)	(ALL)	
AX0*	0	0	1	0	672	666	664	661	666	630	659	655	680	680
AX0*	377	37	376	37	680	689	700	702	683	658	672	689	695	683
AX1	10	1	12	1	655	664	669	667	666	637	667	617	681	686
AX1	367	36	365	36	725	752*****	772	752	730	739	764	723	708	
AX2	22	4	26	4	662	667	681	675	684	645	669	670	689	692
AX2	355	33	351	33	677	683*****	689	683	645	666*****	694	695		
AX3*	61	13	71	13	670	670	677	667	672	634	672	672	687	687
AX3*	316	24	306	24	678	677	677*****	673	644	672	670	683	684	
AX4*	140	7	160	7	675	677	687	667	681	650	672	672	694*****	
AX4*	237	30	217	30	683	689	686	683	683	650	683	686	695	691
AX5	300	14	340	14	673	678	684	675	680	644	680	675	687*****	
AX5	77	23	37	23	741	775	752	752	756	736	706	769	727	784
AX6	204	16	304	16	667	677	683	672	683	645	672	677	683	683
AX6	173	21	73	21	672	630	689	692	692	652	675	686	686	692
AX7	24	11	224	11	675	678	680	670	681	644	672	672	691*****	
AX7	353	26	153	26	689	694	698	691	689	655	683	681	692	695
AY0*	257	2	257	3	661	675	670	667	672	634	661	666	677	680
AY0*	120	35	120	34	683	700	700	700	695	659	683	687	706	706
AY1	360	10	360	12	725	752	752	741	752	727	739	766	728*****	
AY1	17	27	17	25	697	706	706	703	700	666	695	698	697	706
AY2	334	2	334	6	658	659	686	700	670	675	666	703	672*****	
AY2	43	35	43	31	603	622	648	644	706	659	614	614	614	694
AY3	241	5	241	15	578	597	586	592	597	556	589	589	600	600
AY3	136	32	136	22	609	631	614	614	650	636	600	612	606	659
AY4	375	0	375	20	577	600	586	589	580	548	569	583	594*****	
AY4	2	37	2	17	572	577	583	578	614	550	562	575	589	614

#### 4.3.4 Failure List

The failure list tabulates the bad memory cells by column and data line (DQ). The number '9999' in this list indicates that no error was found for that particular address. The Sentry will print out up to ten errors, five per memory half.

	(Left Half)		(Right Half)	
	(Col)	(DQ)	(Col)	(DQ)
BAD	0	1	9999	9999
BAD	7	1	9999	9999
BAD	8	0	9999	9999
BAD	9999	9999	9999	9999
BAD	9999	9999	9999	9999



#### 4.3.5 Footer

The footer line restates the device serial number, gives the slice coordinates (which are only important when testing whole slices), and states the bin number (see Table 10). The footer line also gives the VDD power supply standby current and active current (IDDSB and IDDACTIVE, respectively), and the total number of good byte pairs in the memory. The total number of good byte pairs is the sum of the good address byte pairs (26 maximum) and the good additional byte pairs (234 maximum).

4	3	7	30.00E-03	142.0E-03	****	0	0	252	****	****	****
(S/N)	(Slice)	(Bin)	(IDDSB)	(IDDACTIVE)				(No. of			
	Coordinates)	No.)						Good Byte Pairs)			

Table 10. Bin Number Decode.

1 = Continuity Failure	7 = Fail March Pattern
2 = Power Trips	8 = CNRAM Bit(s) Bad
3 = $I_{dd} > 80 \text{ mA}$	9 = Pass March Pattern
4 = $I_{dd} < 2 \text{ mA}$	10 = More Than 2 Bits Bad on Row 0
5 = Pipe Bit Bad	11 = Repairable
6 = Not Used	12 = Catastrophic Failure

#### 4.4 DATA LOG EXAMPLES

The following pages contain examples of Sentry 21 test data log printouts for SRAM tests. The ten printouts contain one example of each of the ten different test results we encountered during SRAM testing for the LABCOM program. The test results are characterized by the bin number that appears in the footer line of the printout. Table 10 defines the bin numbers produced by the Sentry. Most of the examples are of unsuccessful tests. The successful tests are labeled as bin 9 for 100% functionality and bin 11 for repairable. All of the other bin numbers describe a type of failure.

##### 4.4.1 Bin 1, Continuity Failure

This bin number is assigned to parts with opens, shorts, and major tri-state failures (Fig. 8). The Sentry halts the test at this point and current levels are not displayed for this bin.

```

STAT3          01-20-87 08:46
TEST PROGRAM   TSRAM      S/N      1

```

```

      1          1
BAD   9999 9999      9999 9999
BAD   9999 9999      9999 9999
BAD   9999 9999      9999 9999
BAD   9999 9999      9999 9999
BAD   9999 9999      9999 9999
      1    4    1    1    9999      9999      **** ****    0 **** **** **** ****

```

Figure 8. Bin 1 example.

#### 4.4.2 Bin 2, Power Trips

Bin 2 indicates that one or more of the power lines is drawing current far above normal levels (Fig.9). This condition does not necessarily mean a short circuit (bin 1) but indicates some other major power drain. The Sentry halts the test at this point and current levels are not displayed for this bin.

```

STAT3          01-20-87 09:49
TEST PROGRAM   TSRAM      S/N      34

BAD   9999 9999      9999 9999
BAD   9999 9999      9999 9999
BAD   9999 9999      9999 9999
BAD   9999 9999      9999 9999
BAD   9999 9999      9999 9999
      34    9    6    2    9999      9999      **** ****    0 **** **** **** ****

```

Figure 9. Bin 2 example.

#### 4.4.3 Bin 3, $I_{dd} > 80$ mA

Bin 3 is similar to bin 2 in that it is an excessive current failure. The difference is that bin 2 looks for gross failures on all power lines while bin 2 catches high current levels of  $I_{dd}$  too small for bin 2 to detect. The Sentry halts the test at this point and current levels are displayed. The IDDSB and IDDACTIVE for the example of Fig. 10 are obviously too high.

```

STAT3          01-20-87  09:38
TEST PROGRAM   TSRAM      S/N      26

```

```

BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
    26    2    5    3  226.0E-03  216.0E-03  **** ****  0 **** **** **** ****

```

Figure 10. Bin 3 example.

#### 4.4.4 Bin 4, $I_{dd} < 2$ mA

The Sentry produces a bin 4 error if  $I_{dd}$  is far too small. This condition is not necessarily an open (bin 1) but causes the part to fail. The Sentry halts the test at this point and current levels are displayed. The footer line of the example in Fig. 11 indicates an IDDSB of -2 mA.

```

STAT3          02-03087  09:28
TEST PROGRAM   TSRAM      S/N      34

```

```

BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
    34    9    6    4 -2.000E-03  128.0E-03  **** ****  0 **** **** **** ****

```

Figure 11. Bin 4 example.

#### 4.4.5 Bin 5, Pipe Bit Bad

A bin 5 error indicates that the pipeline active indicator bit in the SRAM's status register has failed to operate normally. The Sentry halts the test at this point and current levels are displayed. The currents for the example in Fig. 12 are typical values. However, most SRAM's that suffer pipe bit failures draw a greater than typical current.

```

STAT3          01-20-87  10:30
TEST PROGRAM   TSRAM      S/N      61

BAD           0      0      16      0
BAD           0      1      16      1
BAD           0      2      16      2
BAD           0      3      16      3
BAD           0      4      16      4
61           1      9      5  20.00E-03  78.00E-03 ****  29  0 **** **** **** ****

```

Figure 12. Bin 5 example.

#### 4.4.6 Bin 6, Not Used

#### 4.4.7 Bin 7, Fail March Pattern

If the SRAM passes all continuity, tri-state, and control RAM tests, it progresses into the address byte pair search part of the test. The SRAM must suffer five or more cell failures during the address byte pair search to be labeled bin 7. The failures that occur will be included in the failure list. The asterisks that appear in the access time section of the example in Fig. 13 indicate the failures. In most cases, a SRAM that fails the march pattern will have less than the maximum 260 good byte pairs.

#### 4.4.8 Bin 8, CNRAM Bit(s) Bad

CNRAM refers to the SRAM's control registers. These registers are tested immediately after the continuity and tri-state tests. If one or more of the bits in these registers fail, the Sentry halts the test at this point and current levels are displayed. As is the case in the example of Fig. 14, the standby and active currents for a device with CNRAM failures are usually very high.

#### 4.4.9 Bin 9, Pass March Pattern

This bin is assigned to the SRAM's that test 100% functional. The part must pass all continuity, tri-state, CNRAM, and address byte pair search tests. The access times and currents must be within acceptable limits and the device must have the maximum 260 good byte pairs. Fig. 15 is an example of a 100% functional SRAM data log.

#### 4.4.10 Bin 10, More Than Two Bits Bad on Row 0

If the Sentry detects more than two errors on the first row of the memory, it aborts the test at that point. This problem has never been encountered, so there is no example printout.

STAT3 01-20-87 08:49  
TEST PROGRAM TSTRAM S/N 4

AX0*	0	0	1	0	764	797	780	787	778	745	750	775	775	795
AX0*	377	37	376	37	706	695	691	695	683	655	670	692	700	706
AX1	10	1	12	1	666	677	683	675	670	637	658	681	678	681
AX1	367	36	365	36	692	706	706	702	692	689	686	702	700	706
AX2	22	4	26	4	662	667	675	667	669	636	659	672	670	677
AX2	355	33	351	33	672	687	686	687	681	647	662	672	686	689
AX3*	61	13	71	13	675	684	694	686	683	653	664	692	683	694
AX3*	316	24	306	24	686	692	695	692	684	650	672	683	683	695
AX4*	140	7	160	7	667	684	683	678	675	647	666	687	683	691
AX4*	237	30	217	30	675	694	689	706	683	650	672	675	689	695
AX5	300	14	340	14	702	720	731	700	717	678	731	706	695	781
AX5	77	23	37	23	744	787	775	781	764	739	734	761	723	787
AX6	204	16	304	16	667	683	684	678	678	650	659	678	683	684
AX6	173	21	73	21	675	628	689	689	680	656	672	687	689	692
AX7	24	11	224	11	672	678	689	678	675	650	664	678	683	689
AX7	353	26	153	26	681	698	694	692	683	650	667	675	687	695
AY0*	257	2	257	3	672	687	689	678	681	650	658	675	689	691
AY0*	120	35	120	34	686	695	698	697	689	652	673	689	700	702
AY1	360	10	360	12	722	750	753	761	750	723	731	752*****		
AY1	17	27	17	25	695	702	705	702	700	662	683	700	705	706
AY2	334	2	334	6	658	700	683	695	670	677	662	700	667	700
AY2	43	35	43	31	659	647	653	700	717	672	627	639	634	716
AY3	241	5	241	15	614	675	667	655	636	639	614	644	647	659
AY3	136	32	136	22	603	625	611	612	659	642	600	606	605	659
AY4	375	0	375	20	573	600	584	591	580	567	566	580	597	600
AY4	2	37	2	17	569	578	580	591	620	567	555	570	587	620
BAD	0	0		31	3									
BAD	0	1		9999	9999									
BAD	0	2		9999	9999									
BAD	0	3		9999	9999									
BAD	1	0		9999	9999									
4	7	2	7	36.00E-03	136.0E-03	****	0	0	259	****	****	****		

Figure 13. Bin 7 example.

STAT3 01-20-87 09:36  
TEST PROGRAM TSTRAM S/N 25

BAD	0	0	16	0								
BAD	0	1	16	1								
BAD	0	2	16	2								
BAD	0	3	16	3								
BAD	0	4	16	4								
25	1	5	8	134.0E-03	202.0E-03	****	0	0	****	****	****	****

Figure 14. Bin 8 example.

STAT3  
TEST PROGRAM

TSRAM

10:35  
S/N 6

AX0*	0 0	1 0	839	819	847	838	858	834	830	845	867	867
AX0*	377 37	376 37	831	836	842	836	853	828	830	844	863	863
AX1	10 1	12 1	822	819	841	833	850	828	831	844	859	858
AX1	367 36	365 36	820	823	834	825	844	822	825	841	853	853
AX2	22 4	26 4	822	819	839	833	852	833	831	845	859	859
AX2	355 33	351 33	822	823	839	833	844	816	828	838	861	863
AX3*	61 13	71 13	819	809	834	822	845	816	809	836	850	850
AX3*	316 24	306 24	822	823	842	838	850	816	839	848	850	850
AX4*	140 7	160 7	823	816	839	833	850	825	836	845	861	861
AX4*	237 30	217 30	839	839	844	844	889	867	856	886	902	891
AX5	300 14	340 14	822	812	839	830	850	828	827	842	861	861
AX5	77 23	37 23	844	838	847	839	855	833	838	850	866	866
AX6	204 16	304 16	819	809	833	828	847	825	828	838	853	853
AX6	173 21	73 21	844	833	847	839	853	825	838	850	866	866
AX7	24 11	224 11	805	816	844	825	850	823	828	842	861	859
AX7	353 26	153 26	827	828	839	833	850	827	834	842	856	856
AY0*	257 2	257 3	809	800	830	817	839	816	809	830	848	848
AY0*	120 35	120 34	819	833	842	833	850	816	833	844	853	853
AY1	360 10	360 12	819	805	833	820	848	819	812	839	850	850
AY1	17 27	17 25	828	839	850	820	855	833	836	853	855	855
AY2	334 2	334 6	809	766	736	747	752	730	737	748	784	809
AY2	43 35	43 31	822	781	728	747	750	747	723	741	769	822
AY3	241 5	241 15	787	769	730	736	750	720	731	742	775	786
AY3	136 32	136 22	839	791	734	750	755	750	730	744	772	836
AY4	375 0	375 20	839	797	737	750	758	747	733	745	773	839
AY4	2 37	2 17	805	764	733	736	741	739	713	739	750	805
BAD	9999 9999	9999 9999										
BAD	9999 9999	9999 9999										
BAD	9999 9999	9999 9999										
BAD	9999 9999	9999 9999										
BAD	9999 9999	9999 9999										
6	5	2	9	18.00E-03	92.00E-03	****	0	0	260	1	0	0

Figure 15. Bin 9 example.

#### 4.4.11 Bin 11, Repairable

To be classified as repairable, an SRAM must pass all continuity, CNRAM, and tri-state tests and progress into the address byte search. The part must suffer no more than four cell failures out of 72K to be labeled repairable. In some cases, a repairable bar will have no errors listed in the error list. The example in Fig. 16 does list one cell error. Most repairable bars will have the maximum 260 good byte pairs but may have as few as 256.

STAT3	02-03087		08:32											
TEST PROGRAM	TSRAM		S/N		1									

AX0*	0	0	1	0	892	900	903	900	914	878	898	895	878	914
AX0*	377	37	376	37	886	895	908	900	912	889	891	897	919	917
AX1	10	1	12	1	891	900	905	900	917	880	898	897	880	917
AX1	367	36	365	36	883	883	886	891	905	870	886	880	867	908
AX2	22	4	26	4	850	820	859	822	873	817	844	836	847	866
AX2	355	33	351	33	891	898	906	900	912	873	897	886	881	912
AX3*	61	13	71	13	880	891	900	897	903	873	892	884	870	903
AX3*	316	24	306	24	867	870	886	877	898	856	869	878	900	897
AX4*	140	7	160	7	886	898	905	902	912	877	900	891	878	912
AX4*	237	30	217	30	867	856	887	864	891	853	870	850	859	880
AX5	300	14	340	14	886	898	908	903	914	881	900	891	880	914
AX5	77	23	37	23	886	891	914	891	914	873	897	889	867	902
AX6	204	16	304	16	887	897	905	900	909	877	900	886	873	909
AX6	173	21	73	21	891	891	908	898	914	886	895	889	905	914
AX7	24	11	224	11	887	900	903	900	925	817	905	900	873	925
AX7	353	26	153	26	844	809	827	808	828	797	805	808	836	856
AY0*	257	2	257	3	873	878	889	883	900	859	878	878	859	897
AY0*	120	35	120	34	873	867	889	884	891	867	887	880	852	891
AY1	360	10	360	12	877	889	908	808	903	880	889	889	870	908
AY1	17	27	17	25	855	856	878	856	886	842	861	863	891	889
AY2	334	2	334	6	766	772	769	773	781	752	767	773	753	783
AY2	43	35	43	31	844	798	758	787	752	758	723	706	711	850
AY3	241	5	241	15	770	761	758	762	769	744	758	764	747	770
AY3	136	32	136	22	838	795	741	752	747	741	727	714	716	844
AY4	375	0	375	20	870	822	775	792	770	764	752	728	747	872
AY4	2	37	2	17	791	770	767	770	780	750	762	769	750	792

1	1													
BAD	9999	9999		24	5									
BAD	9999	9999		9999	9999									
BAD	9999	9999		9999	9999									
BAD	9999	9999		9999	9999									
BAD	9999	9999		9999	9999									

1	4	1	11	14.00E-03	80.00E-03	****	0	0	260	****	****	****
---	---	---	----	-----------	-----------	------	---	---	-----	------	------	------

Figure 16. Bin 11 example.

#### 4.4.12 Bin 12, Catastrophic Failure

For the Sentry to label an SRAM a catastrophic failure, almost all of the cells in the memory must fail. The part will pass the continuity, CNRAM, and tri-state tests but suffer many failures during the address byte pair search. The example of Fig. 17 shows many asterisks instead of access times in the access time section, indicating a large number of failures. The failure list starts at column 0, row 0 and contains the maximum number of errors it can show. Finally, the SRAM in this example has only 20 out of 260 good byte pairs.

STAT3	01-20-87		10:27	
TEST PROGRAM	TSRAM		S/N 60	

AX1	367 36	365 36	1075*****	1062*****	919*****
AX2	22 4	26 4	775 800 891*****		
AX2	355 33	351 33	*****838*****		
AX3*	61 13	71 13	*****		
AX3*	316 24	306 24	734*****	736 728 736*****	725 727 747*****
AX4*	140 7	160 7	***** 728***** 700 716 717*****		
AX4*	237 30	217 30	***** 722 734*****		
AX5	300 14	340 14	783 805 816 819 808 770 798 805 750 819		
AX5	77 23	37 23	***** 814*****		
AX6	204 16	304 16	*****		
AX6	173 21	73 21	892*****	792*****	
AX7	24 11	224 11	*****		
AX7	353 26	153 26	*****		
AY0*	257 2	257 3	*****		
AY0*	120 35	120 34	***** 791***** 752*****		
AY1	360 10	360 12	1055 917*****	798*****	
AY1	17 27	17 25	*****		
AT2	334 2	334 6	***** 706*****		
AY2	43 35	43 31	*****		
AY3	241 5	241 15	***** 698*****		
AY3	136 32	136 22	*****		
AY4	375 0	375 20	*****		
AY4	2 37	2 17	594 600 600 603 628 567 580 600 614*****		
BAD	0 0	16 0			
BAD	0 1	16 1			
BAD	0 2	16 2			
BAD	0 3	16 3			
BAD	0 4	16 4			
60	1 8 12	26.00E-03	136.0E-03	****	0 0 20 **** **** ****

Figure 17. Bin 12 example.

#### 4.5 FUNCTIONAL TEST DATA FOR DELIVERED MODULE

The following pages contain the Sentry 21 test data log printouts produced during the testing of the 32K x 9 VHSIC SRAM module delivered to LABCOM. Each printout contains the data log representing the test of one SRAM of the X4 module.

The first four data logs were produced on 10 January 1987 during the first substrate level functional test of the four SRAM's mounted together on the thick-film interconnect. The second group of four data logs was produced on 13 January 1987 with LABCOM witnessing the test. This test was conducted at the same assembly level as the first test. The third group of data logs was produced on 20 January 1987. This test was performed on the module after the interconnect had been bonded into the 196-lead package. The package had not



been sealed at this point. The final group of data logs was produced on 27 January 1987. This test was performed on the module after the package lid had been seam welded onto the package seal ring. This test was the final test performed on the module before shipping.

All of the data logs from these tests show that the four SRAM's in the module tested 100% functional all four times they were tested. The chip-select access times dropped dramatically between the substrate level tests and the module level tests. For the module level tests, the unit is placed in a socket that is mounted to the DUT board on the Sentry 21 test head. Therefore, there is no longer an access time delay caused by the cabling between the test head, the probe station, and the probe card. Otherwise, the access times are consistent for each SRAM from test to test. On all of the data logs, the failure lists contain only '9999' which means no failures were found. All of the data logs show the bin number 9. Table 10 in Section 4.3.5 defines bin number 9 as "PASS MARCH PATTERN" which means that the SRAM's passed all tests. In all tests, the standby current (IDDSB) is measured to be 84 mA, which is four times a typical value of 21 mA for a single SRAM. The active current (IDDACTIVE) varies from 174 mA to 180 mA depending on the SRAM being tested. This value is typical for 3 SRAM's in standby mode ( $3 * 21 \text{ mA}$ ) and one SRAM in active mode (118 mA). Finally, the data logs state that all the SRAMs have 260 good byte pairs, which is the maximum number possible.

#### 4.5.1 First Substrate Level Functional Test

10 January 1987

```

STAT3                      11:15
TEST PROGRAM                S/N      1

AX0*  0  0      1  0      1000  859  858  850  852  830  842  850  859  1002
AX0* 377 37     376 37     994  847  858  841  850  825  847  842  864  994
AX1   10  1      12  1     1003  873  848  845  844  819  836  844  855  1003
AX1  367 36     365 36     983  850  852  847  850  823  842  842  864  866
AX2   22  4      26  4     1002  858  853  845  848  830  833  848  858  1000
AX2  355 33     351 33     994  844  850  839  850  825  848  844  863  992
AX3*  61 13      71 13     1003  872  855  845  852  828  838  848  855  1003
AX3* 316 24     306 24     853  845  852  838  856  825  847  841  853  856
AX4* 140  7     160  7     1003  973  847  852  847  825  839  852  856  1003
AX4* 237 30     217 30     850  850  853  844  863  833  852  847  873  875
AX5  300 14     340 14     1002  981  844  848  845  827  936  848  845  1002
AX5   77 23      37 23     850  848  855  842  850  828  845  839  853  855
AX6  204 16     304 16     1002  877  845  850  848  820  830  844  850  1000
AX6  173 21      73 21     986  814  847  839  850  817  844  839  858  986
AX7   24 11     224 11     1002  933  850  847  845  820  838  847  847  1002
AX7  353 26     153 26     873  848  848  836  850  822  850  839  853  867
AY0* 257  2     257  3     1006  980  847  842  848  811  836  842  850  1006
AY0* 120 35     120 34     850  845  855  850  853  831  844  847  856  856
AY1  360 10     360 12     1006  975  847  841  848  816  841  848  850  1006
AY1   17 27      17 25     850  847  850  842  852  836  844  844  859  859
AY2  334  2     334  6     1008  986  836  845  800  797  786  780  764  1008
AY2   43 35      43 31     833  811  772  805  794  792  775  784  772  842
AY3  241  5     241 15     1009  969  834  772  794  775  781  770  759  1009
AY3  136 32     136 22     841  758  766  816  792  784  769  772  772  839
AY4  375  0     375 20     1011  881  847  855  787  777  764  778  764  1009
AY4   2 37      2 17      863  809  766  808  787  777  767  781  766  866
1
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
1  4  1  9  84.00E-03  176.0E-03 ****  0  0  260 **** **** ****

```

Figure 18. First substrate level functional test - SRAM number 1.

10 January 1987

STAT3

11:16

TEST PROGRAM

TSRAM

S/N

2

AX0*	0	0	1	0	1012	877	855	859	866	842	853	863	866	1012
AX0*	377	37	376	37	1000	859	861	850	867	836	850	850	867	1000
AX1	10	1	12	1	1012	891	847	850	850	830	842	853	856	1012
AX1	367	36	365	36	864	858	859	850	869	838	861	853	867	870
AX2	22	4	26	4	1011	878	850	855	863	833	845	856	859	1011
AX2	355	33	351	33	1000	858	858	850	870	836	850	850	870	873
AX3*	61	13	71	13	1012	892	850	858	855	836	850	858	863	1012
AX3*	316	24	306	24	859	855	859	850	867	836	853	850	864	869
AX4*	140	7	160	7	1012	900	850	866	859	834	845	856	864	1012
AX4*	237	30	217	30	861	863	864	855	873	839	858	855	873	873
AX5	300	14	340	14	1011	905	852	850	856	836	845	852	859	1011
AX5	77	23	37	23	861	859	856	850	866	834	852	850	867	866
AX6	204	16	304	16	1011	892	850	861	855	834	850	852	861	1012
AX6	173	21	73	21	867	791	858	853	859	834	859	850	866	867
AX7	24	11	224	11	1011	892	847	848	850	828	842	850	850	1009
AX7	353	26	153	26	864	858	861	850	866	836	853	853	863	866
AY0*	257	2	257	3	1012	988	850	850	853	830	845	852	856	1012
AY0*	120	35	120	34	861	863	863	850	866	842	856	850	866	866
AY1	360	10	360	12	1014	966	850	852	859	828	847	855	861	1014
AY1	17	27	17	25	863	856	861	850	866	844	852	850	866	866
AY2	334	2	334	6	1014	992	845	855	812	811	781	781	769	1016
AY2	43	35	43	31	848	750	753	769	792	783	775	775	777	848
AY3	241	5	241	15	1019	911	845	766	802	775	770	767	762	1019
AY3	136	32	136	22	847	750	755	778	789	777	769	758	781	842
AY4	375	0	375	20	1020	892	853	867	789	772	767	775	769	1019
AY4	2	37	2	17	867	758	748	770	786	769	767	770	770	867
BAD	9999	9999	9999	9999	9999	9999								
BAD	9999	9999	9999	9999	9999	9999								
BAD	9999	9999	9999	9999	9999	9999								
BAD	9999	9999	9999	9999	9999	9999								
BAD	9999	9999	9999	9999	9999	9999								
2	5	1	9	84.00E-03	176.0E-03	****	0	0	260	****	****	****		

Figure 19. First substrate level functional test - SRAM number 2.

10 January 1987

STAT3				11:17										
TEST PROGRAM				TSRAM		S/N		3						
AX0*	0	0	1	0	883	856	855	850	856	836	855	855	852	883
AX0*	377	37	376	37	873	847	853	848	864	836	853	855	855	873
AX1	10	1	12	1	1012	861	845	842	850	830	838	848	848	1012
AX1	367	36	365	36	866	850	853	850	867	841	853	852	852	867
AX2	22	4	26	4	886	855	850	844	850	831	844	850	850	886
AX2	355	33	351	33	870	850	856	850	864	842	850	852	853	870
AX3*	61	13	71	13	1012	861	848	847	852	833	844	850	850	1012
AX3*	316	24	306	24	856	845	863	848	863	833	856	852	850	863
AX4*	140	7	160	7	1012	863	848	850	850	828	839	852	850	1012
AX4*	237	30	217	30	853	853	863	853	866	847	855	858	858	866
AX5	300	14	340	14	1012	856	847	841	852	836	841	850	848	1012
AX5	77	23	37	23	863	852	856	850	866	836	861	853	852	866
AX6	204	16	304	16	1012	863	842	841	850	825	838	850	845	1012
AX6	173	21	73	21	867	781	856	850	859	839	847	856	850	867
AX7	24	11	224	11	1009	861	848	841	847	831	844	850	842	1012
AX7	353	26	153	26	870	845	861	850	861	842	850	853	850	867
AY0*	257	2	257	3	1016	866	850	842	850	820	850	850	844	1016
AY0*	120	35	120	34	850	850	856	850	864	850	852	861	850	864
AY1	360	10	360	12	1016	863	850	842	853	819	847	850	847	1016
AY1	17	27	17	25	856	848	861	850	863	848	855	853	850	863
AY2	334	2	334	6	1017	983	820	836	819	806	745	747	761	1016
AY2	43	35	43	31	853	744	781	767	805	800	791	791	766	853
AY3	241	5	241	15	1020	867	819	750	816	755	742	748	755	1020
AY3	136	32	136	22	850	739	747	786	805	800	777	770	770	850
AY4	375	0	375	20	1017	867	839	850	808	769	748	744	761	1017
AY4	2	37	2	17	870	752	737	769	803	794	780	783	761	870
BAD	9999	9999	9999	9999										
BAD	9999	9999	9999	9999										
BAD	9999	9999	9999	9999										
BAD	9999	9999	9999	9999										
BAD	9999	9999	9999	9999										
3	6	1	9	84.00E-03	178.0E-03	****	0	0	260	****	****	****	****	

Figure 20. First substrate level functional test - SRAM number 3.

10 January 1987

STAT3				11:18												
TEST PROGRAM				TSRAM	S/N	4										
AX0*	0	0		1	0	877	850	841	847	847	831	834	850	842	877	
AX0*	377	37		376	37	867	839	844	833	850	823	844	844	842	867	
AX1	10	1		12	1	1012	859	833	838	836	819	828	844	842	1012	
AX1	367	36		365	36	859	838	841	834	850	823	844	844	841	859	
AX2	22	4		26	4	880	853	839	839	842	825	831	850	838	881	
AX2	355	33		351	33	863	842	848	839	850	823	842	844	845	864	
AX3*	61	13		71	13	1016	863	838	842	841	825	830	848	836	1016	
AX3*	316	24		306	24	850	841	844	838	850	822	844	839	839	855	
AX4*	140	7		160	7	1012	863	841	850	841	827	830	850	839	1012	
AX4*	237	30		217	30	848	847	848	839	853	827	847	844	847	853	
AX5	300	14		340	14	1012	864	838	838	839	820	827	844	833	1012	
AX5	77	23		37	23	850	839	847	836	850	823	841	842	839	850	
AX6	204	16		304	16	886	859	836	841	839	822	825	845	834	883	
AX6	173	21		73	21	863	781	841	839	844	828	838	845	836	863	
AX7	24	11		224	11	1012	859	838	839	834	816	825	842	830	1009	
AX7	353	26		153	26	864	839	844	833	848	819	838	842	838	866	
AY0*	257	2		257	3	1017	867	834	839	841	814	827	844	831	1017	
AY0*	120	35		120	34	845	842	847	839	850	825	842	844	839	850	
AY1	360	10		360	12	1017	863	839	839	842	820	828	850	834	1017	
AY1	17	27		17	25	850	839	847	838	850	825	839	842	839	850	
AY2	334	2		334	6	1017	983	817	836	828	809	734	739	758	1017	
AY2	43	35		43	31	850	744	736	755	775	770	745	736	761	850	
AY3	241	5		241	15	1023	870	811	750	825	750	734	736	752	1023	
AY3	136	32		136	22	844	739	742	769	797	755	741	744	767	844	
AY4	375	0		375	20	880	863	839	850	816	750	737	739	759	880	
AY4	2	37		2	17	858	727	730	758	800	745	733	734	759	859	
BAD	9999	9999		9999	9999											
BAD	9999	9999		9999	9999											
BAD	9999	9999		9999	9999											
BAD	9999	9999		9999	9999											
BAD	9999	9999		9999	9999											
4	7	2		9		84.00E-03	180.0E-03	****	0	0	260	****	****	****		

Figure 21. First substrate level functional test - SRAM number 4.

#### 4.5.2 Second Substrate Level Functional Test, LABCOM Witness

13 January 1987

```

STAT3                      01-13-87 10:29
TEST PROGRAM    TSTRAM      S/N      17

AX0*  0  0      1  0      1000  877  866  869  863  838  850  850  870  1000
AX0* 377 37     376 37     991  863  863  853  863  836  850  847  877  991
AX1   10  1      12  1     1002  873  850  859  850  831  842  848  866  1002
AX1  367 36     365 36     984  867  859  859  858  833  848  845  877  986
AX2   22  4      26  4     1000  870  858  858  855  836  841  850  867  1000
AX2  355 33     351 33     988  866  853  852  858  834  852  847  873  986
AX3*  61 13      71 13     1005  994  859  856  863  838  845  850  866  1005
AX3* 316 24     306 24     984  863  856  850  869  838  850  845  867  984
AX4* 140  7     160  7     1003  997  850  864  855  839  848  858  866  1003
AX4* 237 30     217 30     986  869  859  856  873  841  861  850  886  986
AX5  300 14     340 14     1002  997  850  858  852  834  842  850  853  1002
AX5   77 23      37 23     988  864  859  853  863  839  850  844  867  988
AX6  204 16     304 16     1000  991  850  855  856  836  836  848  858  1000
AX6  173 21      73 21     988  825  850  852  858  825  848  844  869  988
AX7   24 11     224 11     1002  994  853  850  853  831  845  850  855  1000
AX7  353 26     153 26     986  867  850  850  861  830  856  845  867  986
AY0* 257  2     257  3     1002  992  850  856  852  827  841  842  861  1002
AY0* 120 35     120 34     986  863  859  859  863  839  850  850  869  986
AY1  360 10     360 12     1002  995  850  850  856  831  847  850  861  1002
AY1   17 27      17 25     988  863  853  850  861  844  850  850  870  986
AY2  334  2     334  6     1005  997  834  850  798  800  787  787  775  1005
AY2   43 35      43 31     980  808  794  828  800  791  780  789  781  980
AY3  241  5     241 15     1006  878  834  773  794  787  767  784  770  1006
AY3  136 32     136 22     983  769  784  833  798  787  773  784  783  983
AY4  375  0     375 20     1011 1000  848  864  787  781  747  787  777  1011
AY4   2 37      2 17      977  812  786  833  794  778  773  787  777  977
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
17   8   4   9 84.00E-03 176.0E-03 **** 0   0 260 **** **** ****

```

Figure 22. Second substrate level functional test - SRAM number 1.

13 January 1987

```
STAT3          01-13-87 10:30
TEST PROGRAM   TSTRAM      S/N      18

AX0*  0  0      1  0      1011 886 863 877 873 852 861 867 875 1011
AX0* 377 37     376 37     1000 878 864 863 880 844 858 853 880 1000
AX1   10  1      12  1      1012 878 850 863 859 844 850 858 867 1012
AX1  367 36     365 36      998 875 867 864 881 847 869 859 880 1000
AX2   22  4      26  4      1009 877 855 867 870 844 852 863 870 1011
AX2  355 33     351 33     1000 878 866 866 883 844 856 853 883 1000
AX3*  61 13      71 13      1016 889 852 863 864 847 853 863 873 1016
AX3* 316 24     306 24      995 872 867 864 880 850 861 853 875 995
AX4* 140  7     160  7     1014 1000 853 873 869 848 852 861 873 1016
AX4* 237 30     217 30      997 881 870 870 884 845 866 859 886 997
AX5  300 14     340 14     1011 1000 858 867 866 845 850 858 870 1012
AX5   77 23      37 23      998 878 863 867 877 844 861 856 880 998
AX6  204 16     304 16     1012 886 853 864 864 847 855 856 870 1011
AX6  173 21      73 21      998 802 863 869 870 839 866 850 875 998
AX7   24 11     224 11     1012 1000 850 863 855 842 850 856 863 1011
AX7  353 26     153 26      997 877 869 863 877 847 861 856 875 998
AY0* 257  2     257  3     1011 998 853 867 863 842 850 853 866 1011
AY0* 120 35     120 34     1000 880 867 866 875 850 863 858 877 1000
AY1  360 10     360 12     1012 1000 855 869 867 842 850 858 870 1012
AY1   17 27      17 25      998 873 866 866 875 850 858 853 875 997
AY2  334  2     334  6     1014 1000 847 783 802 816 770 787 780 1016
AY2   43 35      43 31      989 770 772 794 800 781 778 783 787 992
AY3  241  5     241 15     1017 886 845 762 797 798 761 780 775 1017
AY3  136 32     136 22      994 773 770 795 795 780 770 775 792 994
AY4  375  0     375 20     1020 1003 859 867 792 773 752 787 781 1020
AY4   2 37      2 17      988 762 767 781 791 770 770 781 781 988
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
18   7   4   9 84.00E-03 174.0E-03 **** 0   0 260 **** **** ****
```

Figure 23. Second substrate level functional test - SRAM number 2.

13 January 1987

```

STAT3                      01-13-87 10:31
TEST PROGRAM    TSRAM      S/N      19

AX0*   0  0      1  0      1005  873  866  869  869  847  863  859  866  1005
AX0*  377 37     376 37      994  867  859  863  870  844  859  863  870  994
AX1   10  1      12  1      1006  867  853  855  861  838  845  850  858  1006
AX1  367 36     365 36      983  869  861  863  877  850  861  859  867  986
AX2   22  4      26  4      1000  863  856  858  859  842  850  852  859  1000
AX2  355 33     351 33      989  870  864  864  873  850  855  863  869  989
AX3*   61 13      71 13      1008  870  850  856  864  842  850  859  861  1008
AX3*  316 24     306 24      983  866  866  864  870  847  863  859  866  983
AX4*  140  7     160  7      1005  869  856  861  863  839  848  855  859  1003
AX4*  237 30     217 30      986  875  869  869  875  850  863  866  872  986
AX5   300 14     340 14      1006  866  850  855  864  844  850  856  858  1006
AX5   77 23      37 23      986  873  863  863  875  848  866  861  869  986
AX6  204 16     304 16      1006  863  850  850  859  836  847  850  853  1006
AX6  173 21      73 21      986  841  861  863  867  847  850  863  859  986
AX7   24 11     224 11      1006  870  850  850  855  839  850  850  852  1006
AX7  353 26     153 26      983  866  866  866  870  850  859  861  861  983
AY0*  257  2     257  3      1006  877  853  855  861  831  855  850  855  1006
AY0*  120 35     120 34      986  869  863  863  875  852  861  869  864  986
AY1  360 10     360 12      1005  873  855  855  863  836  852  852  855  1006
AY1   17 27      17 25      983  866  866  863  870  852  863  863  863  983
AY2  334  2     334  6      1011 1000  823  834  819  808  750  750  772  1011
AY2   43 35      43 31      983  833  792  786  816  803  798  794  775  983
AY3  241  5     241 15      1012  873  819  739  809  755  750  764  767  1012
AY3  136 32     136 22      983  769  792  800  812  802  770  783  783  983
AY4  375  0     375 20      1012  877  839  859  797  762  752  752  775  1012
AY4   2 37      2 17      975  777  786  777  812  794  781  791  773  978
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
19   6  4   9  84.00E-03 178.0E-03 ****  0  0  260 **** **** ****

```

Figure 24. Second substrate level functional test - SRAM number 3.



13 January 1987

```

STAT3                      01-13-87 10:32
TEST PROGRAM  T1SRAM      S/N      20

AX0*  0  0      1  0      1006  870  850  863  856  844  844  856  852  1006
AX0* 377 37     376 37     992  859  850  850  863  831  850  848  853  989
AX1   10  1      12  1     1008  864  841  850  845  831  839  847  847  1008
AX1 367 36     365 36     986  855  848  850  858  831  850  848  850  986
AX2   22  4      26  4     1002  861  847  852  850  838  842  852  850  1002
AX2 355 33     351 33     989  861  853  855  859  831  850  848  855  986
AX3*  61 13      71 13     1009  867  844  853  850  839  839  850  848  1011
AX3* 316 24     306 24     983  859  850  852  858  830  850  845  850  983
AX4* 140  7     160  7     1006  866  850  861  850  841  839  853  850  1006
AX4* 237 30     217 30     986  864  852  855  864  833  852  848  856  986
AX5  300 14     340 14     1006  867  844  852  850  834  834  848  847  1006
AX5   77 23      37 23     986  858  850  852  859  831  848  845  850  986
AX6  204 16     304 16     1006  863  844  850  850  836  836  847  848  1006
AX6  173 21      73 21     986  800  847  852  850  833  844  848  848  986
AX7   24 11     224 11     1008  870  842  850  847  830  833  845  842  1006
AX7  353 26     153 26     983  858  850  850  856  828  845  842  850  983
AY0*  257  2     257  3     1006  994  842  852  850  830  836  845  844  1006
AY0* 120 25     120 34     986  856  850  850  855  833  847  845  850  986
AY1  360 10     360 12     1006  873  845  850  850  833  838  850  848  1006
AY1   17 27      17 25     983  856  850  850  853  833  844  844  850  983
AY2  334  2     334  6     1012 1000  819  839  831  798  741  745  770  1011
AY2   43 35      43 31     983  764  789  737  784  761  750  750  772  983
AY3  241  5     241 15     1014  873  811  739  820  752  737  745  767  1016
AY3  136 32     136 22     986  767  778  750  794  756  747  750  778  983
AY4  375  0     375 20     1012  873  842  859  770  753  742  750  775  1014
AY4    2 37      2 17     978  750  739  752  800  750  737  745  772  978
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
20    5    4    9 84.00E-03 180.0E-03 **** 0    0 260 **** **** ****

```

Figure 25. Second substrate level functional test - SRAM number 4.

### 4.5.3 Unsealed Package Test

20 January 1987

```

STAT3                      01-20-87 10:57
TEST PROGRAM    TSRAM      S/N      66

AX0*   0  0          1  0          500 486 500 472 483 469 497 466 500 500
AX0* 377 37        376 37          500 486 506 475 498 469 498 467 502 508
AX1   10  1          12  1          500 478 498 467 489 456 498 462 500 500
AX1 367 36        365 36          500 481 500 483 500 470 502 467 502 502
AX2   22  4          26  4          498 484 500 470 484 470 497 462 500 502
AX2 355 33        351 33          502 492 500 477 491 467 494 462 500 502
AX3*   61 13         71 13          500 480 502 477 481 464 492 464 500 502
AX3* 316 24        306 24          500 489 506 475 500 470 502 467 500 506
AX4*  140  7        160  7          502 481 491 472 483 466 497 458 497 503
AX4* 237 30        217 30          505 494 505 480 487 475 500 472 512 512
AX5  300 14        340 14          500 489 491 464 483 462 500 455 489 500
AX5   77 23         37 23          512 491 511 478 502 478 511 466 497 512
AX6  204 16        304 16          500 478 497 475 480 461 486 458 492 500
AX6  173 21         73 21          506 430 517 475 516 467 505 470 500 517
AX7   24 11        224 11          500 481 498 469 480 459 489 459 497 500
AX7  353 26        153 26          500 483 502 480 502 469 500 467 502 502
AY0*  257  2        257  3          500 478 489 469 486 459 491 464 500 500
AY0* 120 35        120 34          498 491 509 484 508 472 506 472 500 509
AY1  360 10        360 12          500 477 497 470 486 466 498 462 498 500
AY1   17 27         17 25          502 494 502 478 506 478 506 470 503 508
AY2  334  2        334  6          398 381 395 372 400 364 400 362 387 400
AY2   43 35         43 31          442 389 398 383 403 372 400 366 387 442
AY3  241  5        241 15          395 380 389 367 394 359 398 358 383 400
AY3  136 32        136 22          408 398 412 383 414 372 406 370 395 414
AY4  375  0        375 20          400 389 400 375 405 367 402 366 391 405
AY4   2 37         2 17          400 381 397 369 400 361 400 356 383 400
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
66   6   9   9 84.00E-03 176.0E-03 **** 0   0 260 **** **** ****

```

Figure 26. Unsealed package test - SRAM number 1.

20 January 1987

```
STAT3          01-20-87 10:58
TEST PROGRAM   TSRAM          S/N      67

AX0*   0  0      1  0      500 483 491 475 500 472 500 469 514 514
AX0* 377 37     376 37     506 489 503 481 502 475 505 470 516 516
AX1   10  1      12  1     489 475 489 469 484 464 489 462 505 506
AX1 367 36     365 36     506 489 503 483 500 478 500 473 517 519
AX2   22  4      26  4     494 478 494 470 495 470 494 466 509 511
AX2 355 33     351 33     503 495 505 486 500 477 502 475 517 519
AX3*   61 13      71 13     494 481 489 483 495 472 492 466 512 512
AX3* 316 24     306 24     505 494 498 481 498 481 502 473 516 516
AX4*  140  7     160  7     494 480 487 467 492 466 500 467 511 511
AX4* 237 30     217 30     506 498 502 486 500 480 505 478 522 522
AX5  300 14     340 14     498 477 489 470 495 470 498 469 514 514
AX5   77 23      37 23     503 494 500 487 495 475 500 472 516 517
AX6  204 16     304 16     494 475 487 469 497 469 484 464 512 512
AX6  173 21      73 21     508 431 514 483 512 475 500 473 517 517
AX7   24 11     224 11     491 475 483 467 492 467 487 461 508 508
AX7  353 26     153 26     505 497 498 484 497 481 494 475 520 520
AY0*  257  2     257  3     491 481 487 472 497 467 494 464 511 511
AY0* 120 35     120 34     508 494 506 486 500 480 503 473 517 517
AY1  360 10     360 12     491 480 487 473 497 467 494 466 511 511
AY1   17 27      17 25     505 498 498 481 498 480 502 475 519 517
AY2  334  2     334  6     391 378 383 370 395 369 400 366 395 400
AY2   43 35      43 31     436 389 389 380 408 375 403 367 395 436
AY3  241  5     241 15     386 373 381 364 398 364 400 361 391 400
AY3  136 32     136 22     406 397 403 383 417 378 411 373 400 417
AY4  375  0     375 20     400 389 395 377 406 372 405 369 400 406
AY4    2 37      2 17     392 378 389 369 402 364 400 361 389 402
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
  67    7    9    9 84.00E-03 176.0E-03 **** 0    0 260 **** **** ****
```

Figure 27. Unsealed package test - SRAM number 2.

20 January 1987

STAT3		01-20-87 11:00												
TEST	PROGRAM	TSRAM	S/N	68										
AX0*	0 0	1 0	497	472	484	466	478	458	497	455	498	498		
AX0*	377 37	376 37	505	480	587	470	509	467	500	462	500	509		
AX1	10 1	12 1	486	467	477	458	500	452	489	450	489	500		
AX1	367 36	365 36	500	484	489	470	517	469	505	456	500	517		
AX2	22 4	26 4	486	469	475	461	462	453	467	453	497	497		
AX2	355 33	351 33	500	478	498	472	509	475	500	461	500	511		
AX3*	61 13	71 13	486	470	478	466	500	453	491	456	498	500		
AX3*	316 24	306 24	503	486	500	470	505	467	500	461	500	505		
AX4*	140 7	160 7	480	469	477	458	487	452	484	452	492	492		
AX4*	237 30	217 30	508	484	500	478	500	473	497	462	500	508		
AX5	300 14	340 14	491	466	472	456	497	458	486	453	497	497		
AX5	77 23	37 23	506	480	497	475	511	470	502	464	500	511		
AX6	204 16	304 16	491	462	475	456	495	452	484	450	489	497		
AX6	173 21	73 21	505	414	516	473	517	470	502	461	500	517		
AX7	24 11	224 11	481	466	481	458	494	453	491	448	486	494		
AX7	353 26	153 26	502	487	498	470	495	472	494	459	500	502		
AY0*	257 2	257 3	487	464	472	459	487	453	486	450	492	492		
AY0*	120 35	120 34	506	484	495	473	514	475	503	462	500	514		
AY1	360 10	360 12	487	467	478	458	498	453	487	455	495	498		
AY1	17 27	17 25	500	484	500	473	506	473	502	459	500	506		
AY2	334 2	334 6	383	362	364	352	392	353	394	350	383	394		
AY2	43 35	43 31	427	373	367	362	395	361	394	350	381	427		
AY3	241 5	241 15	378	359	362	350	389	350	392	350	378	392		
AY3	126 32	136 22	400	381	386	364	409	362	400	358	392	409		
AY4	375 0	375 20	392	373	277	361	402	358	397	355	387	402		
AY4	2 37	2 17	384	364	366	350	395	350	389	348	375	395		
BAD	9999 9999	9999 9999												
BAD	9999 9999	9999 9999												
BAD	9999 9999	9999 9999												
BAD	9999 9999	9999 9999												
BAD	9999 9999	9999 9999												
68	8	9	9	84.00E-03	173.0E-03	****	0	0	260	****	****	****		

Figure 28. Unsealed package test - SRAM number 3.

20 January 1987

```

STAT3                      01-10-87 11:01
TEST PROGRAM  TSRAM      S/N      69

AX0*  0  0      1  0      472  456  456  450  487  445  459  441  492  492
AX0* 377 37     376 37     481  462  464  450  484  450  464  442  491  491
AX1   19  1      12  1     461  459  459  442  467  437  453  436  486  486
AX1  367 36     365 36     483  461  462  450  470  447  450  444  489  489
AX2   22  4      26  4     466  459  452  444  477  448  450  439  489  491
AX2  355 33     351 33     481  462  464  450  486  442  455  448  495  497
AX3*  61 13      71 13     467  452  456  450  478  450  462  441  487  487
AX3* 316 24     306 24     480  462  461  453  487  448  473  444  492  492
AX4* 140  7     160  7     466  452  452  450  473  447  450  437  486  486
AX4* 237 30     217 30     486  462  462  452  489  450  478  447  497  497
AX5  300 14     340 14     464  452  453  447  481  442  450  439  489  489
AX5   77 23      37 23     481  462  466  450  481  450  470  444  492  494
AX6  204 16     304 16     462  452  452  445  478  442  447  436  486  486
AX6  173 21      73 21     483  408  469  450  481  445  470  444  491  489
AX7   24 11     224 11     461  450  452  447  480  448  450  437  484  484
AX7  353 26     153 26     480  459  464  450  481  450  452  445  495  494
AY0* 257  2     257  3     462  450  450  450  480  442  462  437  487  489
AY0* 120 35     120 34     483  462  466  452  480  450  459  444  492  491
AY1  360 10     360 12     464  450  452  447  481  447  447  442  486  486
AY1   17 27      17 25     480  462  461  450  486  448  461  444  492  494
AY2  334  2     334  6     372  352  353  345  350  347  370  345  380  378
AY2   43 35      43 31     414  367  356  350  353  350  364  345  375  414
AY3  241  5     241 15     367  350  350  342  350  342  370  341  375  375
AY3  136 32     136 22     392  373  370  355  372  350  384  350  386  392
AY4  375  0     375 20     383  367  364  350  364  350  375  348  381  383
AY4   2 37      2 17      375  355  353  345  350  344  375  339  370  375
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
BAD  9999 9999      9999 9999
69   9   9   9  84.00E-03 180.0E-03 ****  0   0 260 **** **** ****

```

Figure 29. Unsealed package test - SRAM number 4.

#### 4.5.4 Final Test of Sealed Package

27 January 1987

STAT3				00:21									
TEST PROGRAM		TSRAM		S/N		4							
AX0*	0 0	1 0	500	487	502	475	486	477	500	470	502	503	
AX0*	377 37	376 37	500	489	508	478	500	477	500	470	509	509	
AX1	10 1	12 1	500	481	500	472	494	466	500	467	503	505	
AX1	367 36	365 36	500	486	502	487	502	478	506	472	508	508	
AX2	22 4	26 4	500	486	502	475	487	477	500	466	503	503	
AX2	355 33	351 33	502	494	502	471	495	475	498	467	506	506	
AX3*	61 13	71 13	500	483	502	481	484	472	497	467	503	503	
AX3*	316 24	306 24	500	491	508	480	505	478	505	470	505	508	
AX4*	140 7	160 7	503	484	494	475	487	473	500	461	500	505	
AX4*	237 30	217 30	506	497	506	484	494	484	505	475	519	519	
AX5	300 14	340 14	502	491	492	467	486	470	500	461	495	502	
AX5	77 23	37 23	512	492	512	481	506	487	514	469	500	514	
AX6	204 16	304 16	500	481	498	478	484	469	492	462	498	500	
AX6	173 21	73 21	506	428	520	480	520	475	509	475	506	520	
AX7	24 11	224 11	500	483	500	473	483	467	494	464	500	500	
AX7	353 26	153 26	500	484	503	484	505	475	502	470	508	508	
AY0*	257 2	257 3	502	481	491	475	487	467	497	467	508	506	
AY0*	120 35	120 34	500	494	511	489	511	480	511	475	505	511	
AY1	360 10	360 12	500	480	498	475	489	472	500	467	500	500	
AY1	17 27	17 25	502	495	503	481	511	586	511	473	509	511	
AY2	334 2	334 6	398	383	395	375	400	370	402	366	395	402	
AY2	43 35	43 31	442	391	400	386	406	378	403	367	394	442	
AY3	241 5	241 15	395	381	391	370	397	367	400	361	389	400	
AY3	136 32	136 22	408	398	412	386	417	380	411	373	400	417	
AY4	375 0	375 20	400	391	400	380	406	373	405	369	398	406	
AY4	2 37	2 17	400	381	398	372	402	367	400	359	389	402	
BAD	9999 9999	9999 9999											
BAD	9999 9999	9999 9999											
BAD	9999 9999	9999 9999											
BAD	9999 9999	9999 9999											
BAD	9999 9999	9999 9999											
4	7	2	9	84.00E-03	176.0E-03	****	0	0	260	****	****	****	

Figure 30. Final test of sealed package - SRAM number 1.

27 January 1987

STAT3		00:23																					
TEST PROGRAM		TSRAM		S/N		5																	
AX0*	0 0	1 0	500	486	494	478	500	480	502	472	520	520											
AX0*	377 37	376 37	506	492	505	486	505	484	511	473	520	520											
AX1	10 1	12 1	491	478	491	473	487	472	495	466	511	511											
AX1	367 36	365 36	508	492	505	487	500	486	506	478	511	511											
AX2	22 4	26 4	495	481	495	473	497	478	498	469	514	514											
AX2	355 33	351 33	505	498	506	491	502	484	508	480	523	523											
AX3*	61 13	71 13	495	484	492	478	498	480	498	469	517	517											
AX3*	316 24	306 24	506	498	500	487	500	487	506	477	522	522											
AX4*	140 7	160 7	495	483	489	472	494	473	500	470	516	516											
AX4*	237 30	217 30	506	500	503	489	500	487	509	481	527	527											
AX5	300 14	340 14	498	481	492	475	498	478	500	473	519	519											
AX5	77 23	37 23	505	497	500	491	498	484	502	475	522	522											
AX6	204 16	304 16	495	480	489	473	498	477	497	469	517	517											
AX6	173 21	73 21	508	430	517	487	517	483	503	477	523	523											
AX7	24 11	224 11	492	478	486	472	492	475	494	464	512	512											
AX7	353 26	153 26	505	500	500	487	500	487	500	480	525	525											
AY0*	257 2	257 3	492	484	489	475	498	475	498	467	517	517											
AY0*	120 35	120 34	508	497	508	491	502	487	509	478	522	522											
AY1	360 10	360 12	492	483	489	477	498	475	498	469	516	517											
AY1	17 27	17 25	505	500	500	486	500	487	506	478	523	523											
AY2	334 2	334 6	392	380	382	372	397	375	403	369	400	403											
AY2	43 35	43 31	436	392	391	383	412	381	406	370	400	436											
AY3	241 5	241 15	387	375	381	367	400	370	400	364	397	400											
AY3	136 32	136 22	406	398	403	386	422	386	414	377	405	422											
AY4	375 0	375 20	400	392	397	380	409	380	408	372	402	409											
AY4	2 37	2 17	392	381	389	370	405	370	402	364	395	406											
BAD	9999 9999	9999 9999																					
BAD	9999 9999	9999 9999																					
BAD	9999 9999	9999 9999																					
BAD	9999 9999	9999 9999																					
BAD	9999 9999	9999 9999																					
5	6	2	9	84.00E-03	176.0E-03	****	0	0	260	****	****	****											

Figure 31. Final test of sealed package - SRAM number 2.

27 January 1987

STAT3				00:24										
TEST PROGRAM	TSRAM			S/N	6									

AX0*	0	0	1	0	497	475	484	470	483	466	500	459	500	500
AX0*	377	37	376	37	505	481	487	473	512	475	502	466	503	512
AX1	10	1	12	1	486	469	478	462	502	459	495	450	497	502
AX1	367	36	365	36	500	487	489	473	520	477	508	461	502	520
AX2	22	4	26	4	487	472	477	466	467	461	473	458	500	500
AX2	355	33	351	33	500	481	498	475	512	481	502	464	502	512
AX3*	61	13	71	13	486	472	480	470	500	461	497	461	500	502
AX3*	316	24	306	24	503	487	500	473	508	473	503	464	502	508
AX4*	140	7	160	7	480	470	478	461	487	459	489	455	498	498
AX4*	237	30	217	30	506	487	500	481	500	481	500	466	505	508
AX5	300	14	340	14	491	467	473	461	498	466	492	458	500	500
AX5	77	23	37	23	508	481	498	478	514	478	506	467	505	514
AX6	204	16	304	16	491	466	477	461	498	456	491	453	495	498
AX6	173	21	73	21	506	412	517	477	520	475	506	464	503	522
AX7	24	11	224	11	483	467	483	462	497	461	497	450	492	497
AX7	353	26	153	26	502	491	498	475	497	480	500	464	505	503
AY0*	257	2	257	3	487	467	473	464	491	461	492	450	498	498
AY0*	120	35	120	34	505	487	497	475	517	483	506	467	502	517
AY1	360	10	360	12	487	469	480	462	500	461	494	459	500	500
AY1	17	27	17	25	500	487	500	478	506	478	506	464	502	508
AY2	334	2	334	6	383	364	364	355	395	359	398	353	389	398
AY2	43	35	43	31	427	375	369	366	395	366	398	353	389	427
AY3	241	5	241	15	380	361	362	350	392	356	397	350	384	397
AY3	136	32	136	22	400	383	386	367	412	369	402	362	398	412
AY4	375	0	375	20	392	275	578	264	405	364	400	358	394	405
AY4	2	37	2	17	384	366	367	353	398	358	394	350	381	398
BAD	9999	9999	9999	9999										
BAD	9999	9999	9999	9999										
BAD	9999	9999	9999	9999										
BAD	9999	9999	9999	9999										
BAD	9999	9999	9999	9999										
6	5	2	9	86.00E-03	178.0E-03	****	0	0	260	****	****	****		

Figure 32. Final test of sealed package - SRAM number 3.



27 January 1987

STAT3			00:25											
TEST	PROGRAM	TSRAM	S/N	7										
AX0*	0 0	1 0	472	461	459	455	491	450	467	445	498	498		
AX0*	377 37	376 37	483	464	467	453	487	453	473	447	498	498		
AX1	10 1	12 1	462	452	450	447	470	445	459	439	492	492		
AX1	367 36	365 36	484	464	466	453	473	450	455	447	495	495		
AX2	22 4	26 4	467	452	455	448	480	453	453	444	497	497		
AX2	355 33	351 33	483	466	467	453	487	452	464	450	500	500		
AX3*	61 13	71 13	467	455	459	450	481	453	467	445	494	494		
AX3*	316 24	306 24	481	466	464	458	491	453	478	447	500	500		
AX4*	140 7	160 7	467	455	456	452	477	452	453	444	494	492		
AX4*	237 30	217 30	486	467	466	456	494	455	483	450	500	500		
AX5	300 14	340 14	466	456	458	450	486	450	453	442	495	497		
AX5	77 23	37 23	483	467	469	455	484	455	475	448	498	498		
AX6	204 16	304 16	464	456	455	450	481	450	450	441	492	492		
AX6	173 21	73 21	483	408	470	453	487	450	475	447	498	498		
AX7	24 11	224 11	462	452	455	450	483	452	458	442	491	491		
AX7	353 26	153 26	480	464	467	453	486	453	459	450	500	500		
AY0*	257 2	257 3	464	453	452	450	484	450	469	441	495	495		
AY0*	120 35	120 34	484	466	469	455	483	455	467	448	498	498		
AY1	360 10	360 12	466	452	455	450	484	453	450	447	494	492		
AY1	17 27	17 25	481	467	464	453	487	452	467	448	500	500		
AY2	334 2	334 6	372	355	355	348	352	350	372	348	386	386		
AY2	43 35	43 31	414	369	359	353	358	353	370	348	383	414		
AY3	241 5	241 15	367	352	350	345	350	348	375	344	381	381		
AY3	136 32	136 22	392	375	370	359	375	358	389	352	392	392		
AY4	375 0	375 20	383	369	366	355	367	353	380	350	387	387		
AY4	2 37	2 17	375	358	355	348	352	350	380	341	378	380		
BAD	9999 9999	9999 9999												
BAD	9999 9999	9999 9999												
BAD	9999 9999	9999 9999												
BAD	9999 9999	9999 9999												
BAD	9999 9999	9999 9999												
7	4	2	9	84.00E-03	180.0E-03	****	0	0	260	****	****	****		

Figure 33. Final test of sealed package - SRAM number 4.

#### 4.6 8K X 9 SRAM TESTING - FINAL YIELD DATA

The following data outlines the yield encountered testing VHSIC SRAM's for the LABCOM-VMC program. The yield data is presented in terms of the percentage of good and repairable bars per slice tested. Also presented are the yields by lot and the overall yield.

It is evident that the yield for these parts is highly lot dependent. Of the two lots we tested, lot 11300 had a far higher yield than did lot 11838. Within each lot, the yield varied widely from slice to slice. For example, within lot 11838, slice 04 had a yield of 50% while slice 26 had a yield of 0%. The slice yields in lot 11300 ranged from 44% to 86%. The overall yield for the program was 35%.

This yield data takes into account all types of failures whether they are caused by wafer fabrication, additional processing, or a bad TAB bond.

##### 4.6.1 Lot 11300 - all bars are on 3M TAB tape

<u>Slice No.</u>	<u>No. of Bars</u>	<u>Good/Rep.</u>	<u>Yield</u>
16	17	7/2	53%
28	11	6/1	64%
36	7	2/4	86%
41	18	0/8	44%
44	6	2/2	67%
Lot Total	59	17/17	58%

##### 4.6.2 Lot 11838 - all bars are on IMI TAB tape

<u>Slice No.</u>	<u>No. of Bars</u>	<u>Good/Rep.</u>	<u>Yield</u>
04	34	9/8	50%
11	18	2/5	39%
12	22	0/1	4.5%
20	35	1/5	17%
26	17	0/0	0%
Lot Total	126	12/19	25%

##### 4.6.3 Overall Yield

<u>No. of Bars</u>	<u>Good/Rep.</u>	<u>Yield</u>
185	19/36	35%

#### 4.7 CHARACTERIZATION TESTING

##### 4.7.1 Contractual Requirements

4.3.9 ELECTRICAL PROPERTIES Critical electrical parameters of the package, with respect to VHSIC device and system performance, shall be optimized to the maximum extent feasible. Package trace resistance, capacitance, and inductance along with ground plane resistance and proximity to signal lines, shall be appropriate to meet VHSIC chip applications with system clock rates of 100 MHz.

##### 5.2 TEST PLAN Special provisions

- a. Electrical characterization of packages including R, L, and C measurements of I/O lead metallization and package insulation resistance.
- b. Electrical characterization of chip interconnect system using VHSIC or VHSIC-like chips.

##### 4.7.2 Summary of Test Sequence

Package characteristics were analyzed by performing two sets of tests. First, an RF characterization was done to verify the 100 MHz operating criterion. These tests were designed to analyze the inductive, capacitive, and resistive effects inherent in the package design. A 26 GHz automatic network analyzer was used to take the measurements and TOUCHSTONE analysis and modeling software was used to predict and manipulate the data.

Second, an analysis was performed on the package power and ground planes to determine the specific characteristics associated with each. These tests were made with a variety of equipment from simple ohmmeters to complex thermal imaging systems. This data is intended to provide package users with relevant information on power delivery through the package.

All tests were performed at 25°C unless otherwise noted, using the procedures called out in Appendix F. The following pages provide the details of the characterization testing data.

#### 4.8 ELECTRICAL CHARACTERIZATION AND MODEL

##### 4.8.1 Introduction

This report details the electrical characteristics of the 196-lead VHSIC multichip package's signal lines. An examination of measured package data is presented, and an R-L-C equivalent circuit is determined which accurately models the package characteristics. To understand the signal-handling characteristics of the package, the effects of the test equipment and test fixture must be isolated from the package. Measured package data can be clouded by poor test fixturing and/or inadequate test equipment. RF connectors and transmission lines must be used in the test fixture in order to minimize the parasitics associated with the measurements. The signal line characterization will include RF characteristics and pulsed signal characteristics.

The development of high-density, high-speed digital integrated circuits must be supported by the application of new techniques and methods of package design. As VHSIC devices become faster, requiring higher frequencies and faster transition times as well as large chip counts, the need for specially designed packages becomes necessary. Currently available flat packs and leadless chip carriers were intended for use with VLSI type devices. Though some have high pin counts, they are intended for use with clock and bit rates of only 1-10 MHz and transition times of 3-5 ns. The VHSIC goals are for frequencies  $> 100$  MHz and transition times  $< 1$  ns. To ensure that the packages used for VHSIC chips will pass the necessary signals without causing unacceptable signal distortion the packages must be treated as transmission line structures by package designers.

#### 4.8.2 Physical Characteristics

In the TI 196-lead VHSIC multichip package special attention was paid to the physical characteristics affecting the electrical behavior of the package. The signal lines are 8 mil wide traces separated by 6 mil gaps. All are formed in a single plane sandwiched above and below by parallel AC ground planes. The key advantage to surrounding the signal traces with ground planes is the ability of these structures to exhibit uniform and controlled impedances. Because all the field lines are contained within the ground plane boundaries, these structures support Transvers Electro-Magnetic (TEM) mode wave propagation, and therefore can be modeled as stripline type transmission lines. Packages which simply provide planar signal traces without AC ground planes do not behave as transmission lines, thus they do not exhibit uniform or controlled impedances. Several different forms of wave guiding structures exist. They are made of parallel metal strips and layers on a dielectric substrate in order to support TEM and quasi-TEM mode wave propagation. Stripline and microstrip will be used in modeling this package.

The package is composed of eight parallel layers, each separated by a 7-mil thick aluminum oxide ( $\text{Al}_2\text{O}_3$ ) dielectric material ( $E_r = 9.6$ ). Starting from the bottom (Fig. 34) the first package layer, the thermal base layer, is composed of a heavy nickel-plated and copper infiltrated tungsten material. Layer 2 (Fig. 35) is the tertiary power plane. Layer 3 (Fig. 36) is the secondary power plane and capacitor pads. Layer 4 (Fig. 37) is the primary power plane. Layer 5 (Fig. 38) is the lower ground plane. Layer 6 (Fig. 39) is composed of the power and ground connections, the signal traces, and the bonding shelf. Layer 7 (Fig. 40) is the upper ground plane. Layer 8 (Fig. 41) contains the I/O lead braze pads and seal ring braze metallization. This top (8th) layer is nickel/gold plated kovar material for the package leads and the seal ring material. All the inner wall conductors (ground, power, signal, via) are tungsten thick-film material. The exposed bond shelf portion of the signal lines is nickel/gold plated tungsten. The signal line plane (Fig. 39) contains 176 signal I/O's, 12 power I/O's, and eight ground pads. Along a single edge of the package, there are 44 signal I/O's, 3 power I/O's, and 2 ground I/O leads. The ground pads (planes) are connected by vertical vias originating in the thermal base layer and passing all the way up to the seal ring metallization.

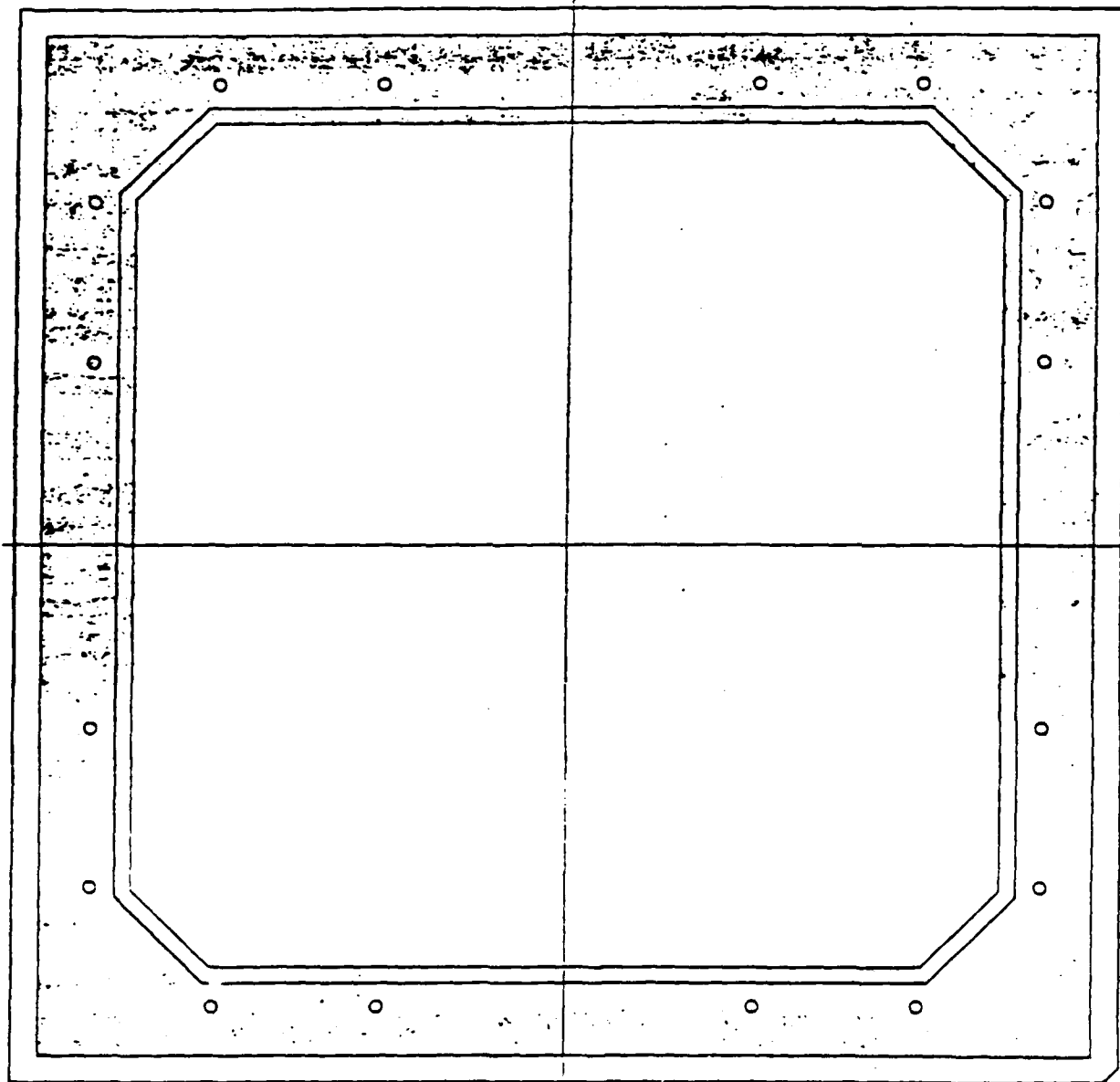


Figure 34. Braze metallization for thermal base attachment.

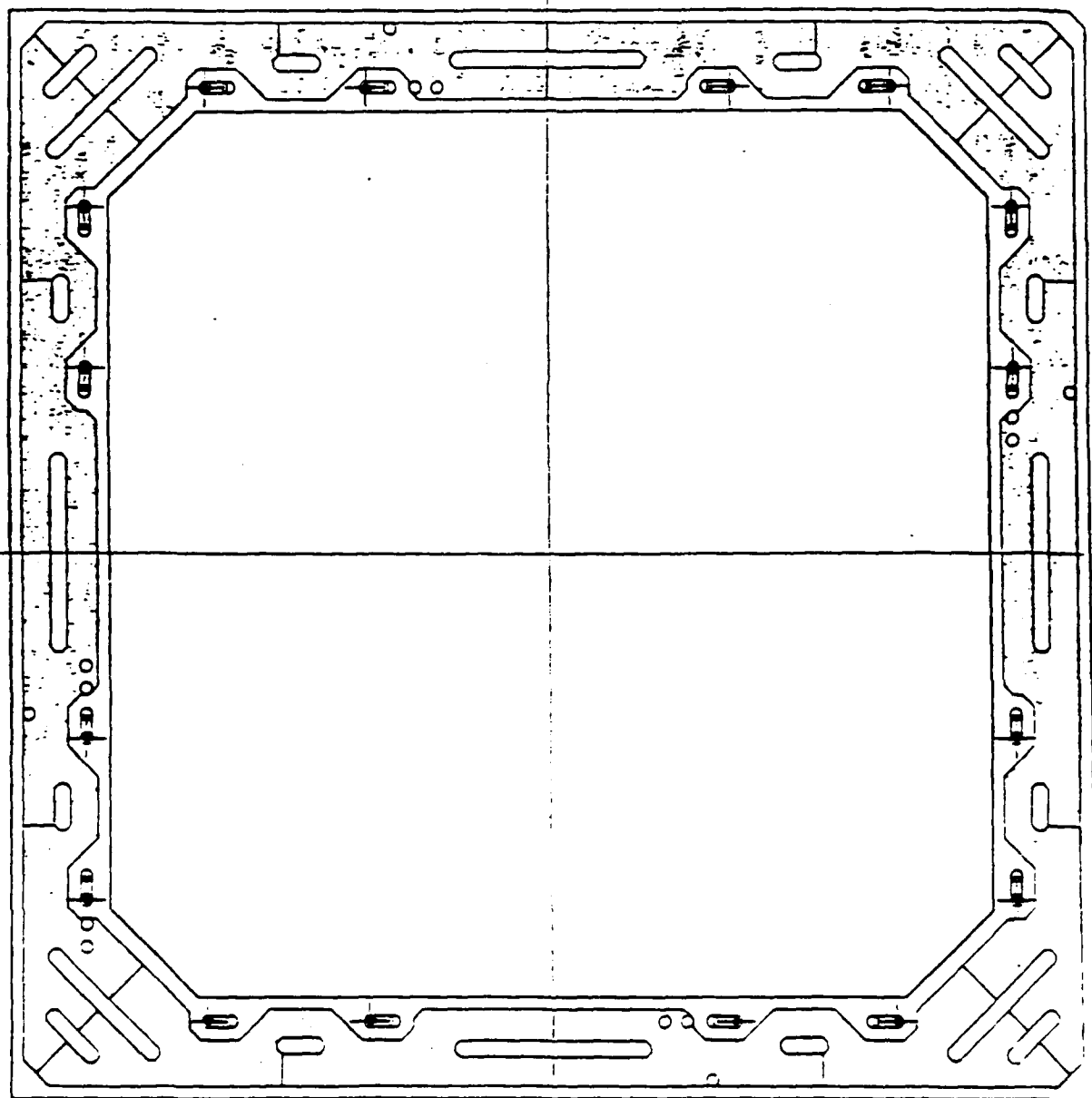


Figure 35. Tertiary power plane.

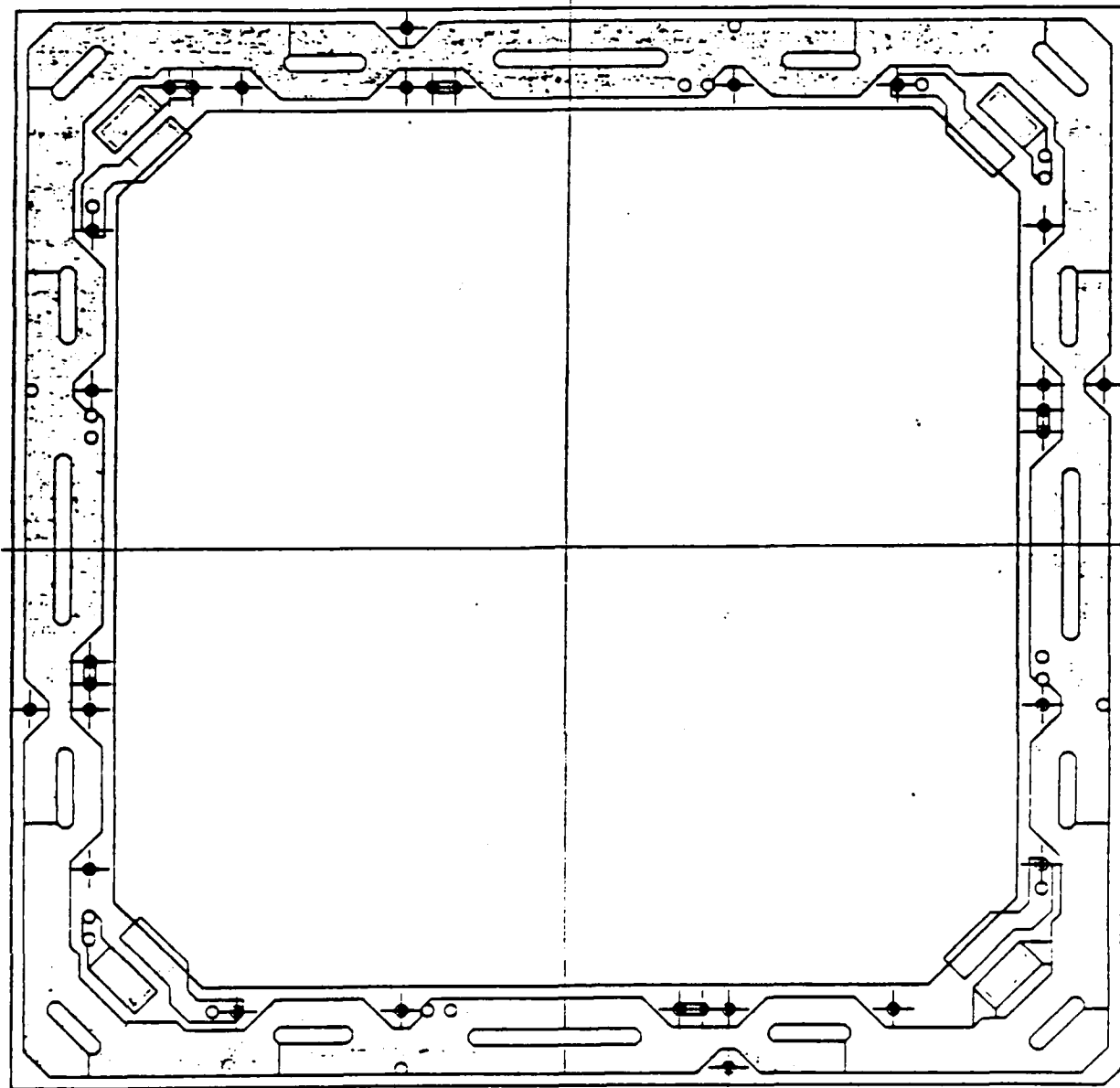


Figure 36. Secondary power plane.

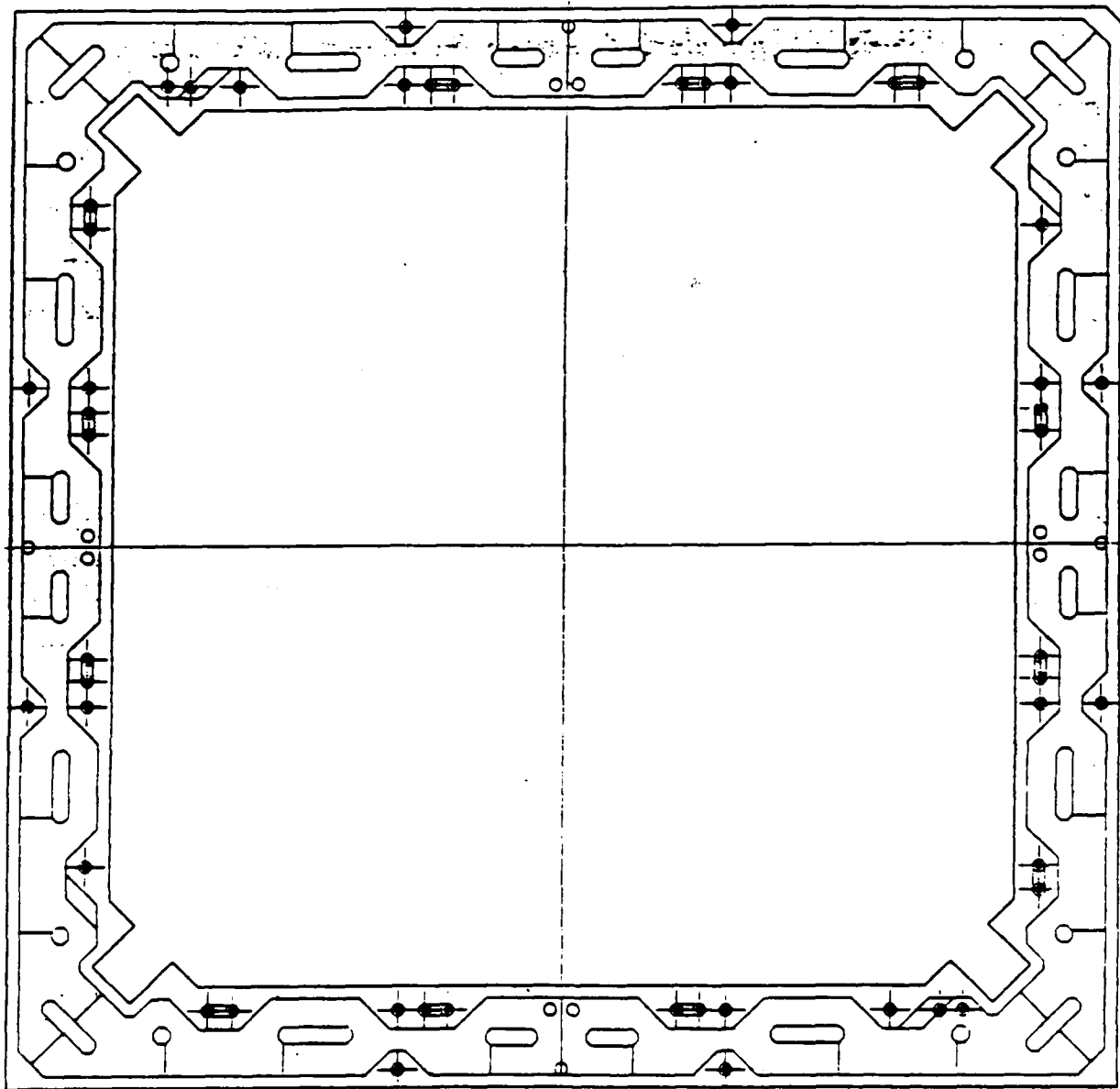


Figure 37. Primary power plane.



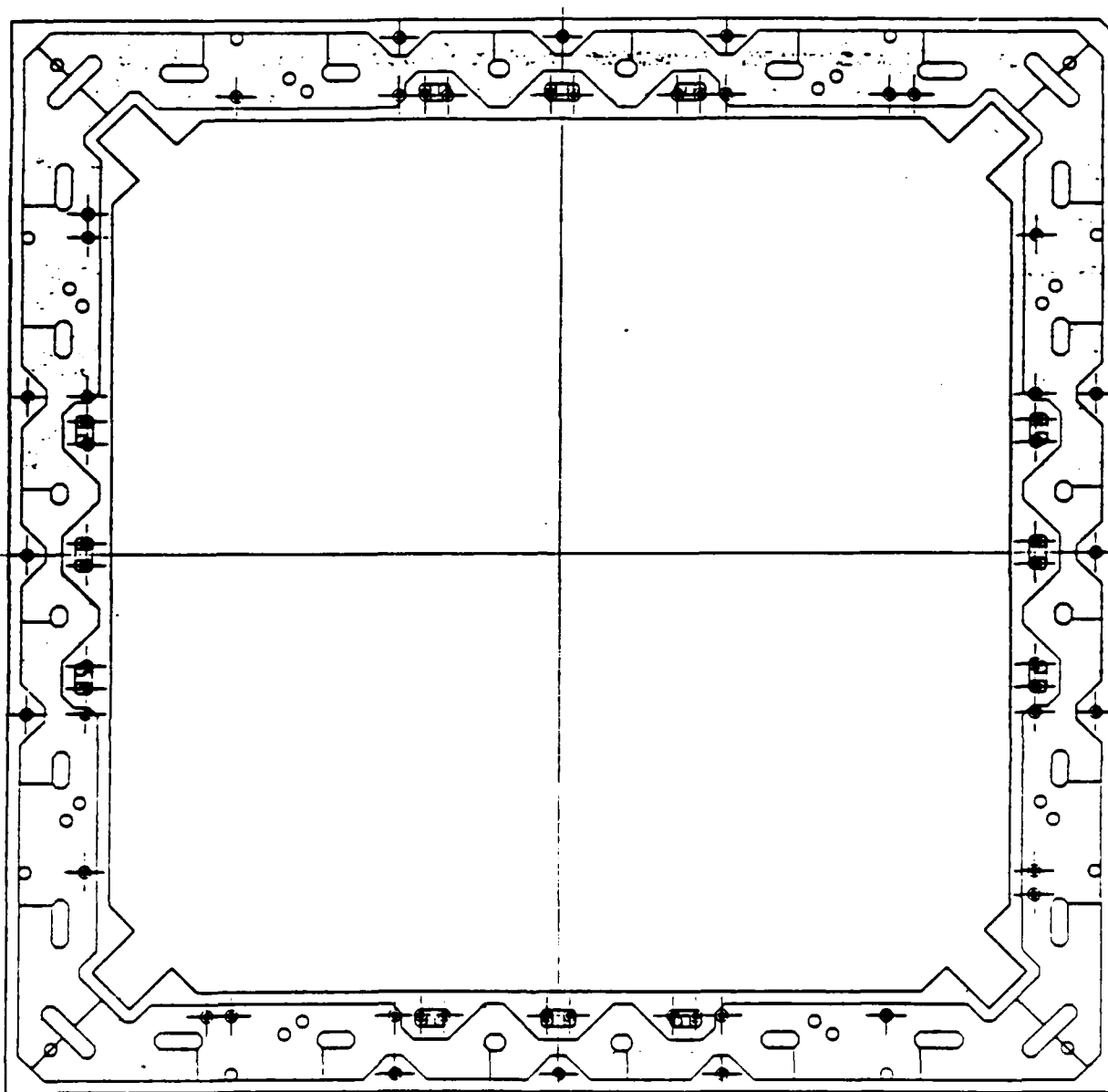


Figure 38. Lower ground plane.

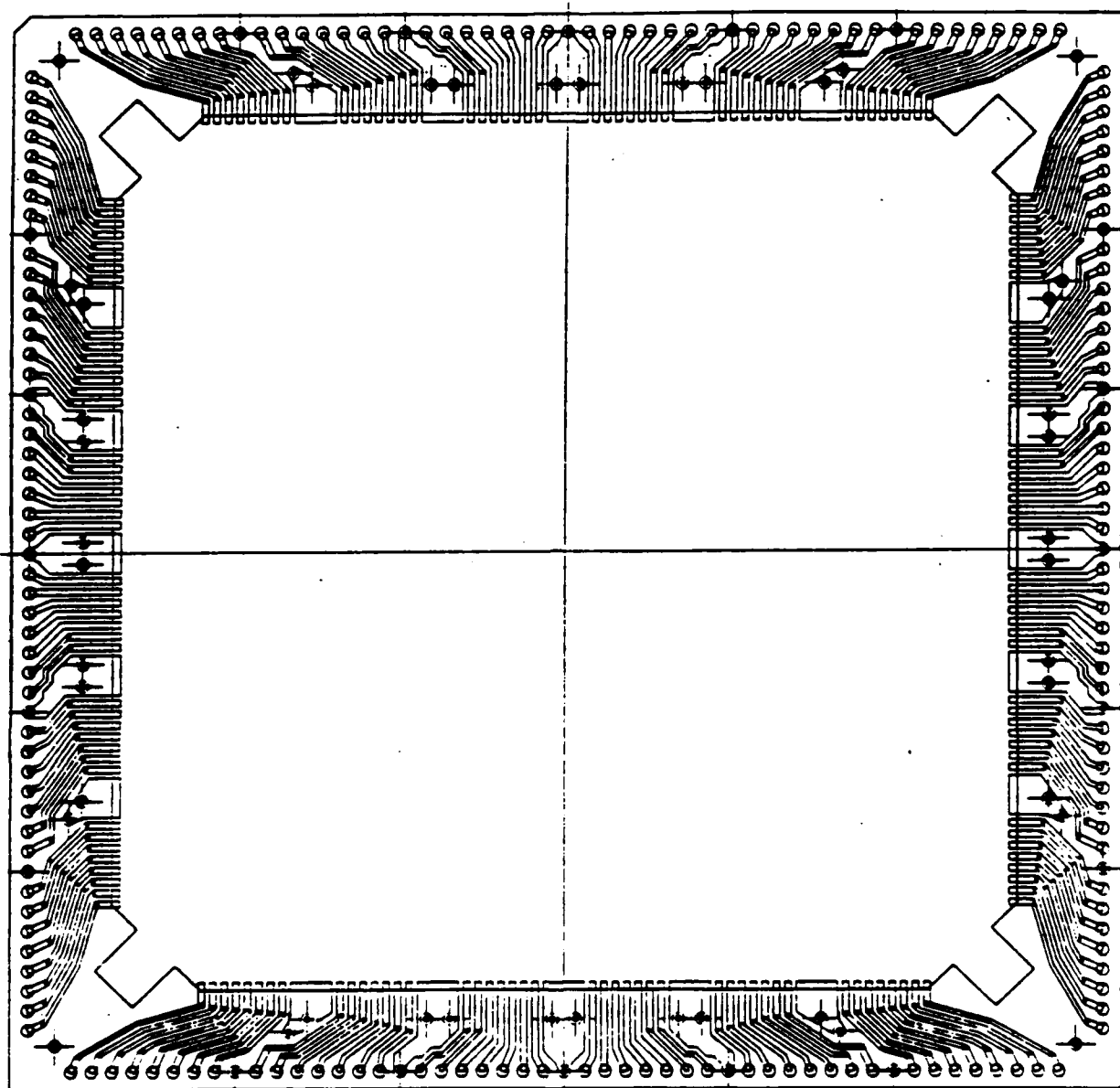


Figure 39. Signal, power and ground connections, bonding shelf.

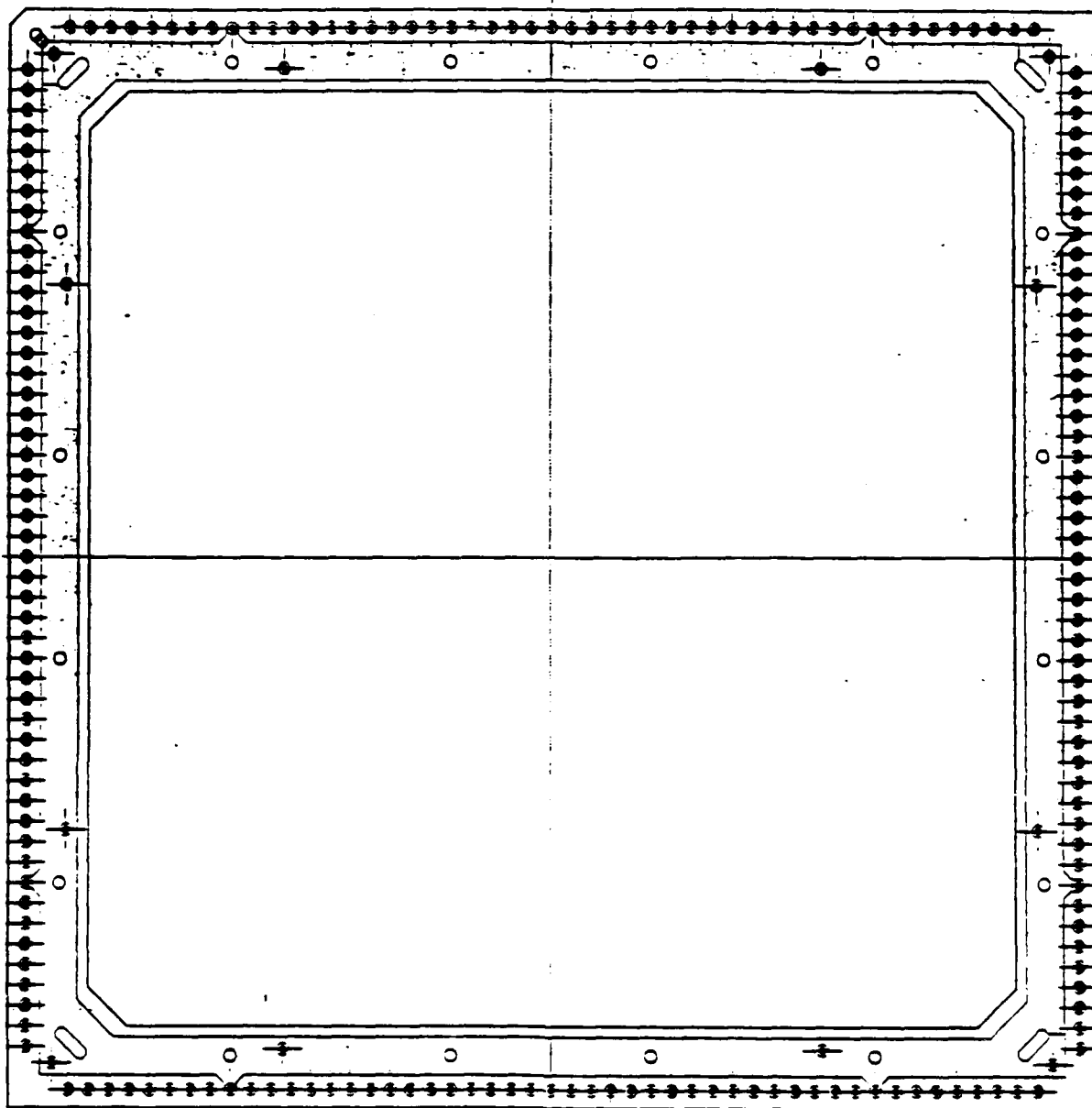


Figure 40. Upper ground plane.

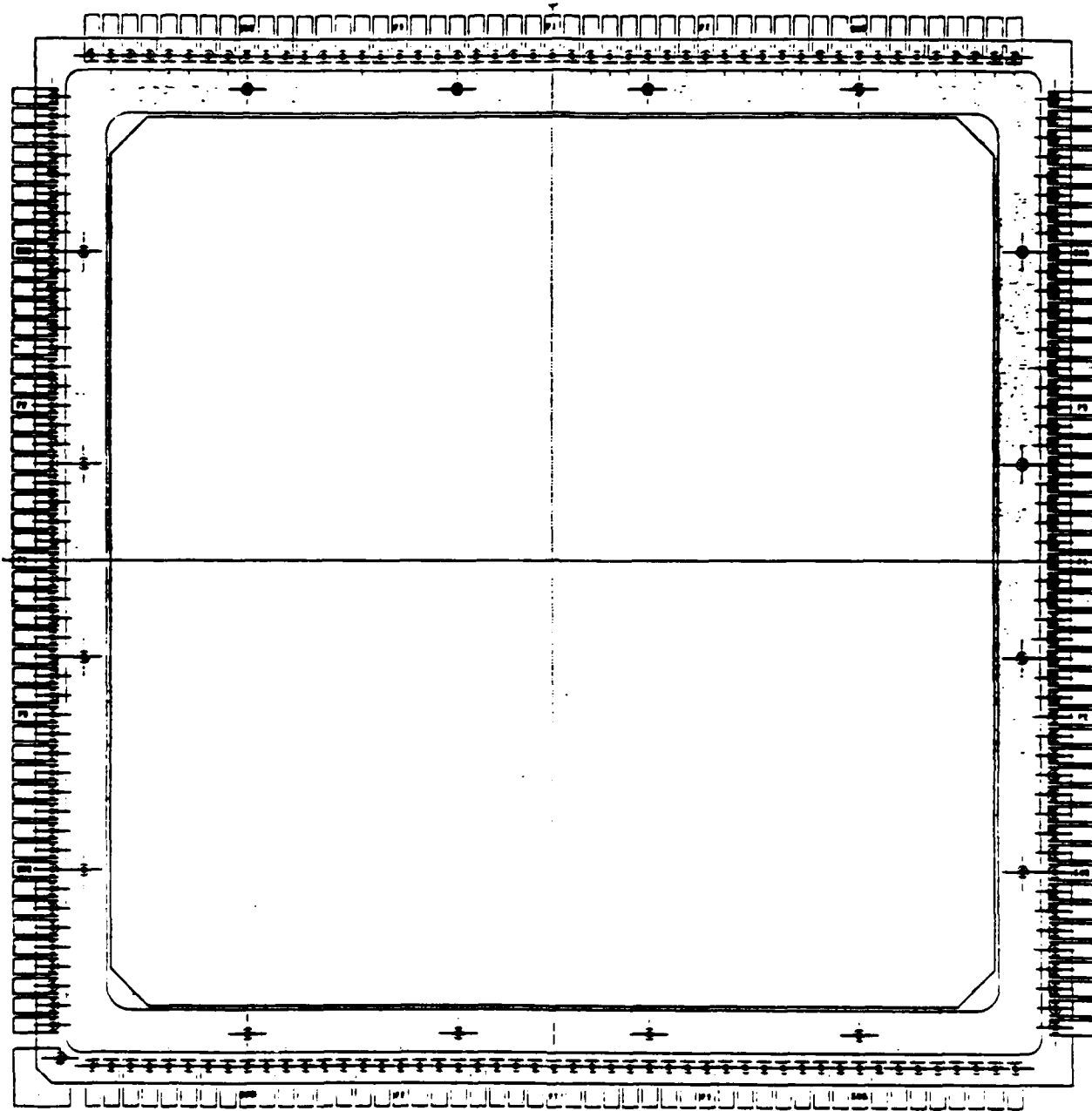


Figure 41. I/O braze pads and seal ring braze metallization.

Each outer edge dimension is 1.22 inches. The signal line trace length (see Fig. 39) varies with position along the perimeter of the package. The shortest traces are located in the center position of the edge, and the signal trace length increases as they progress outward toward the corners of the package. From an electrical point of view, the longer signal traces represent the worst performance case because they have higher insulation resistance, higher series inductance, higher capacitance to ground, and higher coupling capacitance to adjacent signal traces. The propagation delay is also greater in the longer lines. This report will focus on this longest signal line case since it represents the worst case for this package and will always offer poorer electrical performance than the shorter signal lines.

#### 4.8.3 TOUCHSTONE Distributed Element Model

As previously mentioned, the signal line structures can basically be represented as microstrip and stripline transmission lines. The following describes the TOUCHSTONE computer modeling approach with the final element values calculated in a following paragraph. In Fig. 42, a cross-sectional view shows the major sections of the package.

Section 1 (Figs. 41 and 42) has three parts:

1. The lead section is modeled as an inductor in series with some resistance
2. The section of the lead brazed to the top layer of the package functions as a microstrip line because it has a parallel ground plane below it
3. The vertical via functions as a series inductance. The inductance and resistance of the package lead and the via will be lumped together in the computer simulator.

Section 2 (Figs. 39 and 42) contains the internal signal traces. These structures are modeled as striplines due to the parallel ground planes above and below.

Section 3 (Figs. 39 and 42) has bond pads that are microstrip lines with the lower ground plane.

The TOUCHSTONE computer software simulates the transmission line distributed elements and the final R-L-C model elements. The TOUCHSTONE software allows for specification of microstrip and stripline parameters and/or discrete R-L-C parameters. A TOUCHSTONE simulation was used to get a first approximation of the signal line electrical behavior. The physical dimensions of the package will provide the parameters for the microstrip and stripline sections of the model, and the series R and L values will be calculated (Fig. 43 shows the TOUCHSTONE model file).

The plots of Figs. 44 and 45 show the resulting S11 and S21 data respectively. Fig. 44 (S11) is the return loss plotted in dB. The plot shows that the return loss decreases until a deep null is reached, then continues to decrease again as the frequency increases. At 100 MHz the return loss is 32 dB, which corresponds to a 1.05:1 VSWR in the 50-ohm system of the model. In Fig. 45 (S21) the insertion loss gradually increases with increasing frequency. The modeled data of Fig. 45 suggest that a 3 dB cut-off for this package is somewhere above 1 GHz, and at 100 MHz there is less than 0.1 dB insertion loss.

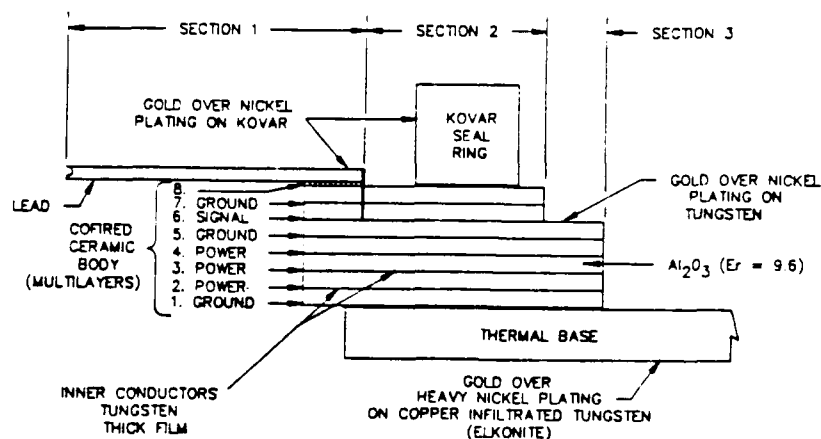


Figure 42. Cross-sectional view of package.

```

CKT
ILABCOM PACKAGE INTERNAL WALL STRUCTURE *** DIM
SSUB  ER=9.6 B=14 T=.5 RHO=1          FREQ MHZ
MSUB  ER=9.6 H=7 T=.5 RHO=1 RGH=0      RES OH
RIBBON 10 20 W=10 L=190 RHO=1          IND NH
MLIN  20 30 W=20 L=30                  CAP PF
WIRE   30 40 D=14 L=14 RHO=1          LNG MIL
SLIN   40 90 W=8 L=150                 TIME NS
MLIN   90 90 W=8 L=25
DEF2P  10 90 PKGIN
TRANSMISSION LINE MOUNTED INSIDE THE PACKAGE ***
WIRE   100 110 D=9 L=75 RHO=1
MSUB  ER=9.6 H=15 T=.5 RHO=1 RGH=0
MLIN  110 120 W=15 L=1075
WIRE   120 130 D=9 L=75 RHO=1
DEF2P  100 130 MIDLINE
TRANSMISSION LINE MOUNTED OUTSIDE PACKAGE ***
MSUB  ER=9.6 H=15 T=.5 RHO=1 RGH=0
MLIN  150 160 W=15 L=363
DEF2P  150 160 START
ILABCOM PACKAGE INTERNAL WALL STRUCTURE (REVERSED) ***
SSUB  ER=9.6 B=14 T=.5 RHO=1
MSUB  ER=9.6 H=7 T=.5 RHO=1 RGH=0
MLIN  200 210 W=8 L=25
SLIN  210 290 W=8 L=150
WIRE   290 260 D=14 L=14 RHO=1
MLIN  260 270 W=20 L=30
RIBBON 270 280 W=10 L=190 RHO=1
DEF2P  200 280 PKGOUT
DISTRIBUTED ELEMENT MODEL OF PACKAGE AND TEST FIXTURE ***
START  1 2
PKGIN  2 3
MIDLINE 3 4
PKGOUT 4 5
START  5 6
DEF2P  1 6 PACKAGE
FREQ
SWEEP 90 1250 20

```

} Test  
Fixture

Figure 43. TOUCHSTONE distributed element model.

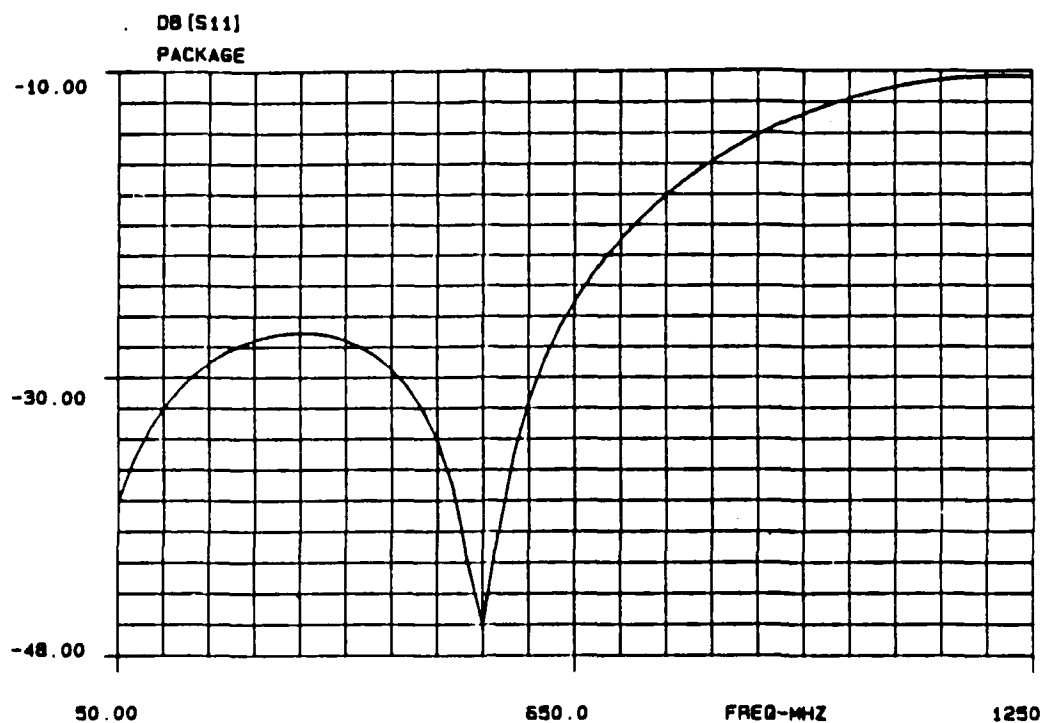


Figure 44. TOUCHSTONE distributed element model (S11).

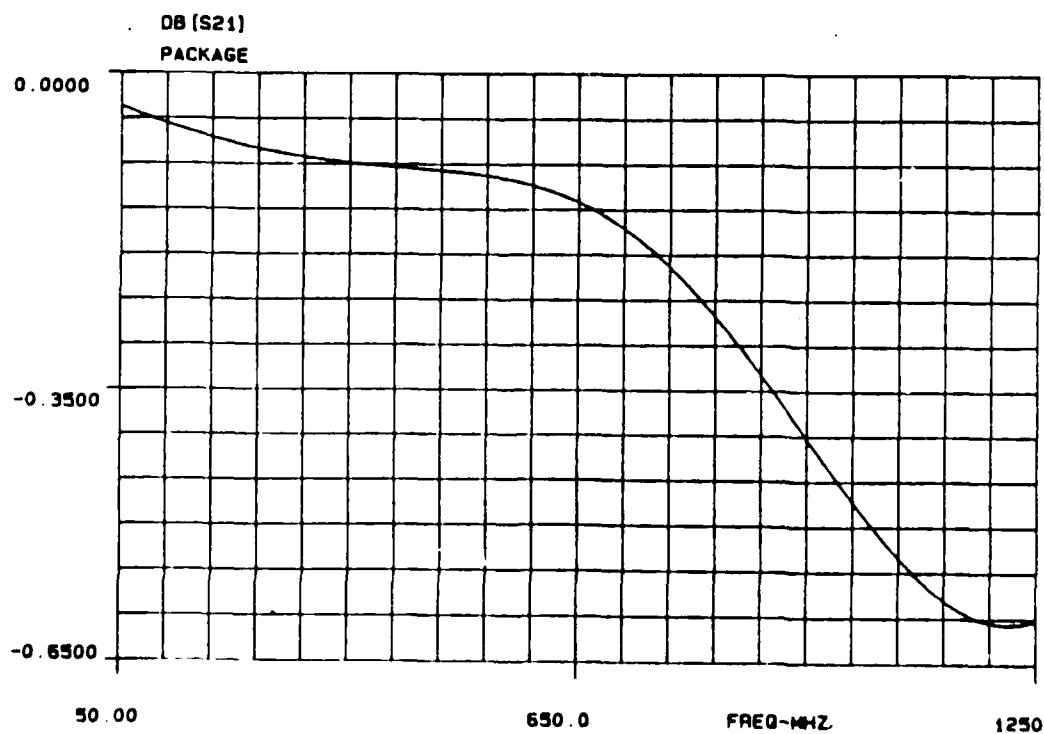


Figure 45. TOUCHSTONE distributed element model (S21).

#### 4.8.4 HP8510 Network Analyzer Measurements

In order to measure the actual package electrical properties, a test fixture allowing direct measurement of the package's signal lines had to be built. Fig. 46 shows the test fixture used to obtain the measured data. The connectors are SMA type, 50-ohm transmission line launchers connected to a section of 50-ohm microstrip line. Conductive epoxy was used to connect the 50-ohm microstrip lines to the package external leads. At the inner bond pad, a 5-mil gold bond wire (25 mil long) connects to another section of 50-ohm microstrip transmission line. Similar connections are made at the opposite side of the package to allow the input signal to propagate completely through the package.

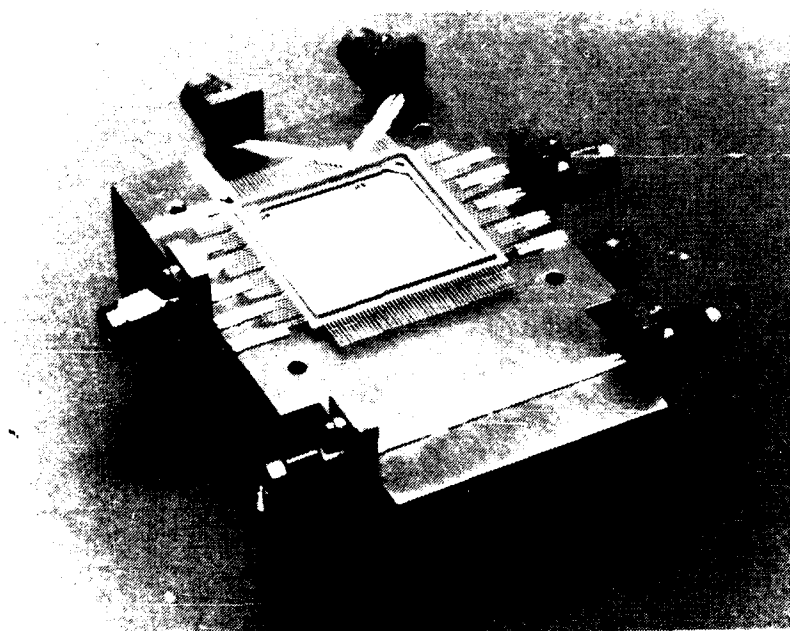


Figure 46. Test fixture used to obtain ANA data.

Fig. 47 shows the test hardware used to obtain the measured data. The HP 8510 network analyzer has a 50-ohm S-parameter test set, thus the 50-ohm connectors and transmission lines were used in the test fixture. The test fixture's SMA connectors allow connection to the test set as shown in Fig. 47. The long section of transmission line between the two SMA connectors, (Fig. 46) was sometimes used during analyzer calibration as the thru standard to calibrate out the losses due to the connectors and the three sections of 50-ohm transmission line in the test fixture.



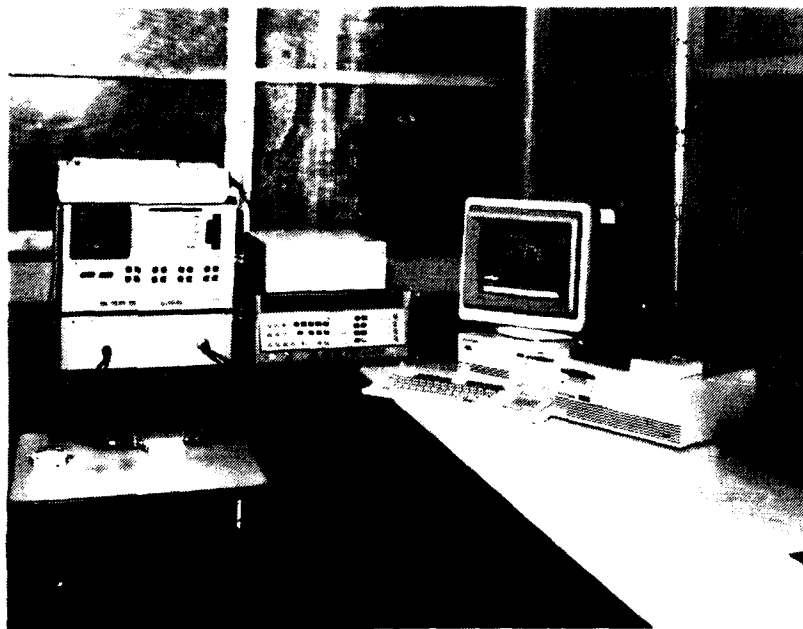


Figure 47. Test hardware used to obtain measured data.

The data obtained from this fixture is a direct measure of the electrical parameters of the package's signal lines. In Fig. 46, the two connectors at the far end of the aluminum block are connected to transmission lines which then connect to package leads of adjacent signal lines. Each of these signal lines is then terminated in 50 ohms inside the package. The adjacent signal lines will provide direct measurements of the coupling from one line to another. They will also allow measurement of the return loss of a signal line terminated with a 50-ohm resistor instead of the transmission line looking into the other side of the package.

Several measurements were made of the package's S21 and S11 using the HP 8510 network analyzer and the test fixture. Measurements were made from 50 MHz to 1250 MHz. Fig. 48 shows the S11 results. These indicate agreement with the distributed element model provided by the TOUCHSTONE software (Fig. 44). Notice in Fig. 43 that the test fixture's 50-ohm transmission line structures are included in the model. The 50-ohm microstriplines were not calibrated out during these measurements.

Where the signal line is terminated with a 50-ohm resistor, the S11 data looks much like the data of Fig. 48 without the null. The null is a result of the forward and reflective standing waves on the signal lines adding constructively at one frequency. Tests showed that for different line lengths the position of the null changes. The transmission data (S21) requires that a return path for the test signal be provided; therefore, the 50-ohm transmission line path will be measured instead of a 50-ohm resistor termination.

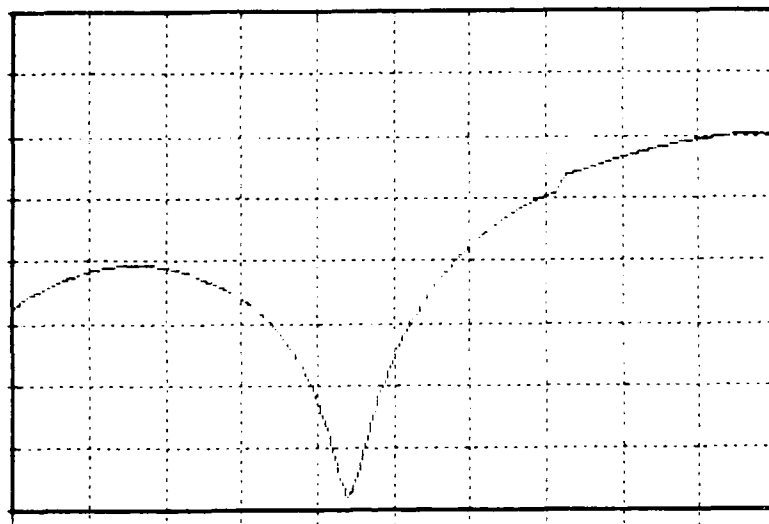


Figure 48. HP 8510 ANA measured S11 results.

Fig. 49 shows the measured insertion loss (S21) for the signal lines. Again, the measured data is in agreement with the TOUCHSTONE model data of Fig. 45. In all the cases presented, the data is very good for a 100 MHz sinusoidal signal in a 50 ohm load condition. At 100 MHz the return loss is down 31 dB - a VSWR of 1.05:1 - and the insertion loss is .2 dB. Also, the TOUCHSTONE distributed model is in agreement with the measured data.

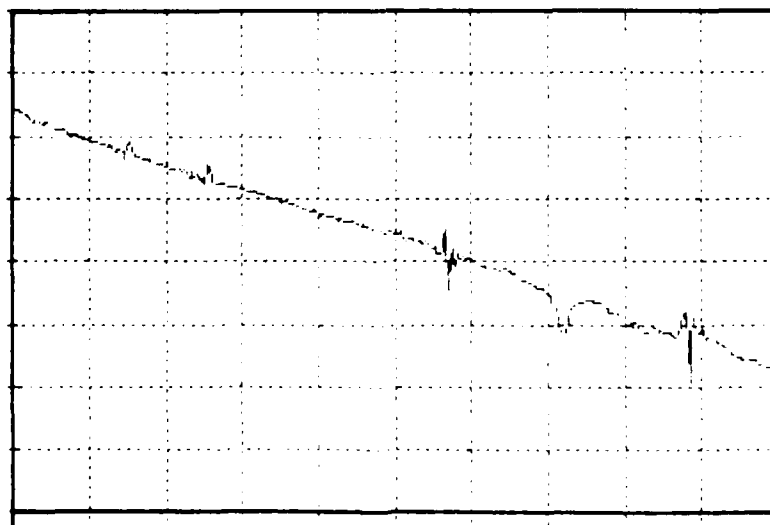


Figure 49. HP 8510 ANA measured S21 results.

#### 4.8.5 Clock Signal Measurements

When digital pulses with  $< 1$  ns transition times are applied to the package, the effect of the high-frequency response becomes important. If a rising or falling edge of a pulse is to be considered an impulse transitioning in zero time, the frequency bandwidth of the network required to transmit this pulse without distortion must be infinite. In real pulses there is a time interval required for the signal to transition from one state to another (rise time and fall time). The faster the transition time, the broader the network bandwidth must be in order to preserve the integrity of the rising and falling edges of the signal. However, for very fast transition times, say 100 ps, it is not necessary that the bandwidth extend into the 10-20 GHz range even though the transition edges may possess harmonics in this range. This is because the higher the frequency harmonic, the less it contributes to the waveform. Some frequencies may be cut off by the network bandwidth, but the signal will suffer only a small (acceptable) level of distortion.

Fig. 50 shows  $S_{11}$  measured from 50 MHz to 12.05 GHz. The return loss is seen to decrease as the frequency increases.

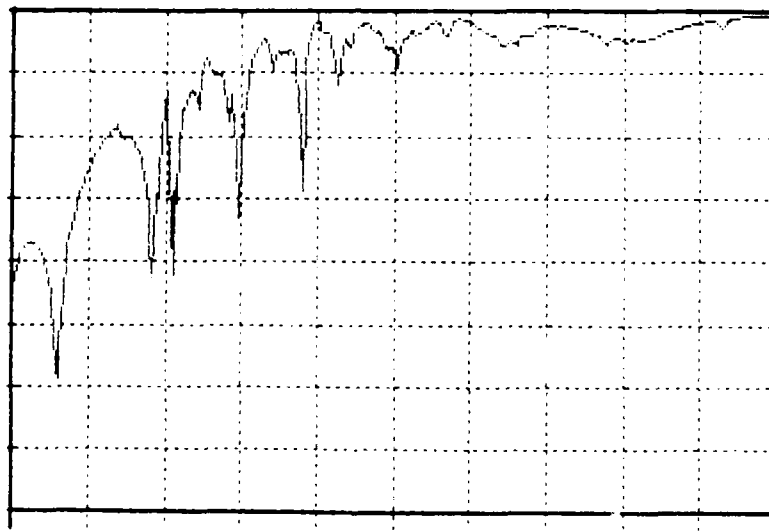


Figure 50. Measured wideband  $S_{11}$  response.

Fig. 51 shows the insertion loss,  $S_{21}$ , for the 50 MHz to 12.05 GHz case. The 3 dB cut-off point occurs at about 3 GHz and the insertion loss continues to roll off as the frequency increases. Bandwidth is just one factor affecting the signals. The mismatch of the load and physical discontinuities along the signal path generate reflections that degrade signal integrity. If the transition time of the signal is greater than or equal to twice (2X) the time delay of the signal trace then no degradation will occur. When twice the signal path delay exceeds the transition time the reflected signal will exist after the transition has finished and will add vectorially to the input signal.

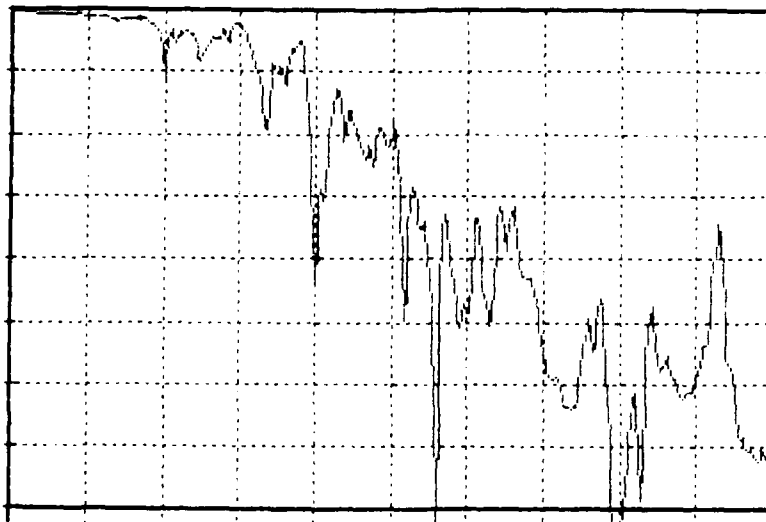


Figure 51. Measured wideband S21 response.

For the 196 I/O LABCOM package, the speed of light is  $c = 3 \times 10^8$  m/s =  $11.811 \times 10^{12}$  mil/s, and the relative velocity inside the package is  $v_p = c/\text{SQRT}(E_r) = 3.811 \times 10^{12}$  mil/s.

For the shortest path length, distance = 300 mil including 200 mil lead; therefore, time delay ( $t_p$ ) = distance/velocity = 78.699 ps and  $2 \times t_p = 157.398$  ps.

For the longest signal path, distance = 350 mil including 200 mil lead; therefore,  $t_p = 91.839$  ps and  $2 \times t_p = 183.678$  ps.

To determine if 100 MHz clock signals with < 1 ns rise times would pass through the package with an acceptable level of distortion (as a result of the limited bandwidth of the package) the package response to such signals was measured. According to the above calculations, the distortion resulting from reflections will not become prominent until transitions of less than 185 ps occur.

The same test fixture used for the ANA frequency domain tests was used to measure the package response to clock signals. The test signals were provided by an HP 8080A pulse generator, and the test waveforms were captured by an HP 54110D digital oscilloscope. Fig. 52 shows a pulse train of 283.286 MHz with 300 ps rise times and 320 ps fall times. This is the oscilloscope display of the test pulses taken directly from the pulse generator. The peak-to-peak voltages of the pulses were 1.152 volts. Fig. 53 shows the pulse train after it has passed through the package. The figure demonstrates that the amount of overshoot, or ringing, is negligible. This is due to two things: 1) the path length is short enough (as shown in the above calculations) that any

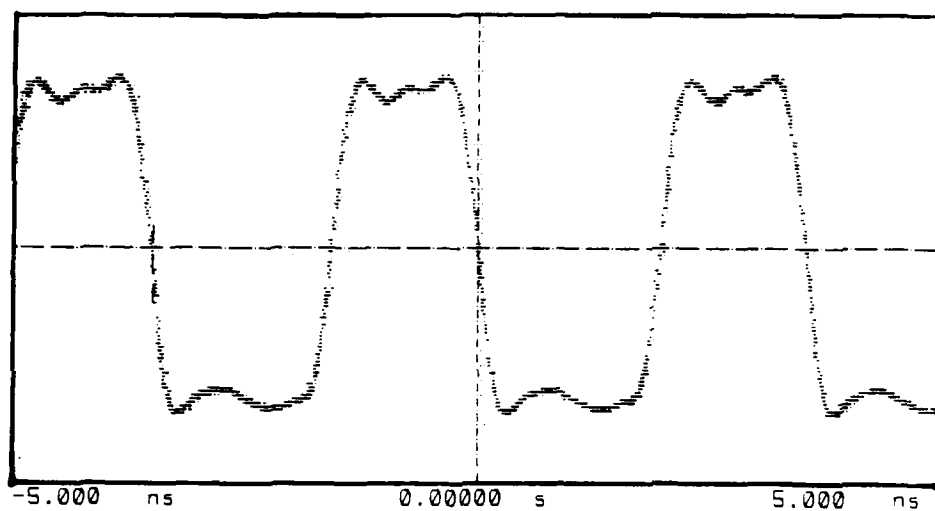


Figure 52. Pulse test signal, 300 ps rise time, 320 ps fall time.

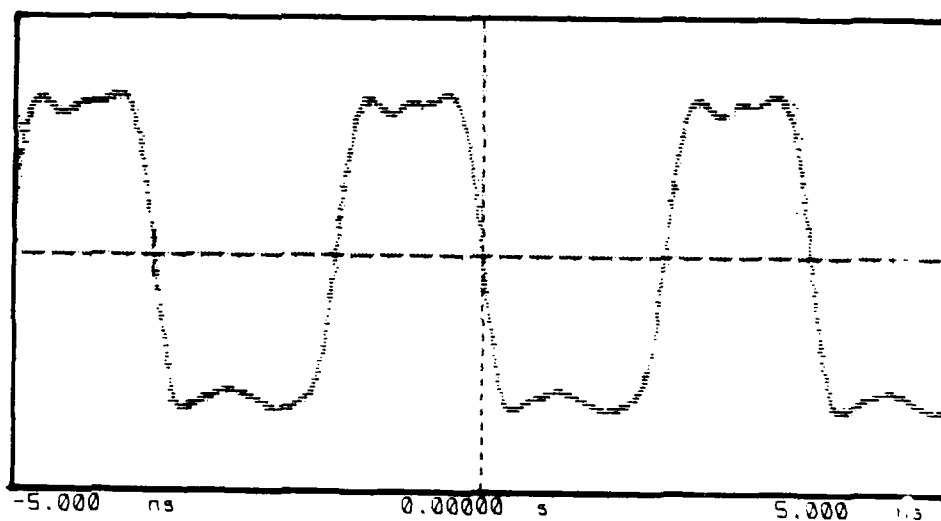


Figure 53. Pulse after passing through package, -0.6 dB insertion loss.

distortion due to reflections is masked during the transition of the test pulse, and 2) the test fixture setup terminates the package in 50 ohms, which provides a high return loss for these signals. The peak-to-peak voltage of the signal after passing through the package is 1.072V equating to an insertion loss of -0.6 dB. The rise time and fall time of the test signals increased approximately 30 ps, due primarily to the limited bandwidth of the package as shown in the frequency response plot of Fig. 51.

The specified response time of the oscilloscope is 350 ps. However, the test signal had a 300 ps rise time which means the usable bandwidth of the oscilloscope is slightly greater than 1 GHz. The package response time (based on the 3 GHz measured 3 dB bandwidth of the package) is  $0.35/(3 \text{ GHz}) = 116 \text{ ps}$ . The combined oscilloscope and package response time is:  $[\text{SQRT}((300)^2 + (116)^2) = 322 \text{ ps}$ , which is approximately what was measured on the test signal after passing through the package. With the test equipment limitations in mind, it is difficult to exactly quantify the contribution made by the package alone. It is clear, however, that the package's signal lines exceed the oscilloscope in usable bandwidth. The measured data indicates that signals with approximately 116 ps transition times and greater will pass through the package with very little distortion if the lines are matched to the source and load. Distortion of the transition edges of the signal caused by reflections at the load will not become prominent until the signal transition time drops below 184 ps, although load mismatch will result in an increase in the insertion loss of the signal. Since package designers cannot make (as an integral part of the package) a dynamic matching circuit for every VHSIC device mounted in the package 50 ohms was chosen for this package to accommodate a general range of impedances.

#### 4.8.6 Cross Talk

In order to maintain a small footprint yet achieve a high I/O count, the adjacent signal traces were run very close together. The signal traces are 8 mil wide, and the gaps between adjacent signal lines are 6 mil. Fig. 39 shows that the trace separation increases to greater than 6 mil near the outer edge of the package. If the separation between signal lines is sufficiently small, and the distance to ground planes sufficiently large, capacitive and inductive coupling will occur between adjacent signal lines. An example of this can be seen in Fig. 54, which shows the theoretical frequency and time domain behavior of capacitively coupled microstrip lines. Worst-case coupling will occur when the victim line is terminated in a matched impedance; in this case, 50 ohms. Fig. 54 shows the coupling as an exponential function of frequency. In the time domain for clock signals, the coupling is greatest at the rising and falling edges, because these transition points represent very high frequencies when transition times less than 1 ns are present.

Using the HP 8510 ANA and the test fixture, the coupling as a function of frequency was measured. Fig. 46 shows that the test fixture connectors on the far end of the test block are set up to measure coupling of adjacent leads terminated in 50 ohms. The results in Fig. 55 clearly show an exponentially increasing dependence on frequency. It can be seen from the figure that at 100 MHz there is approximately -31 dB of coupling, and at 1 GHz there is -14 dB coupling.

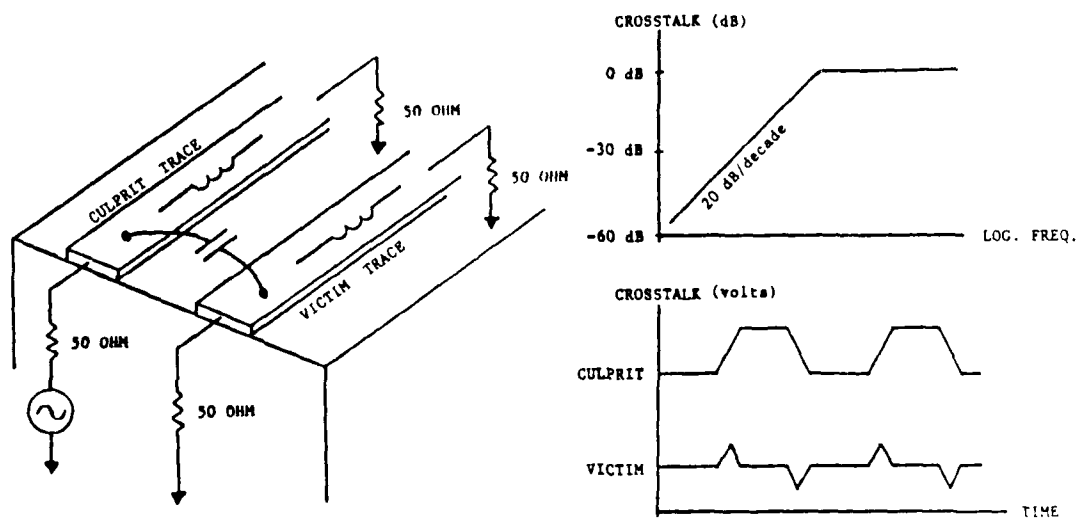


Figure 54. Theoretical cross talk for coupled microstrip lines.

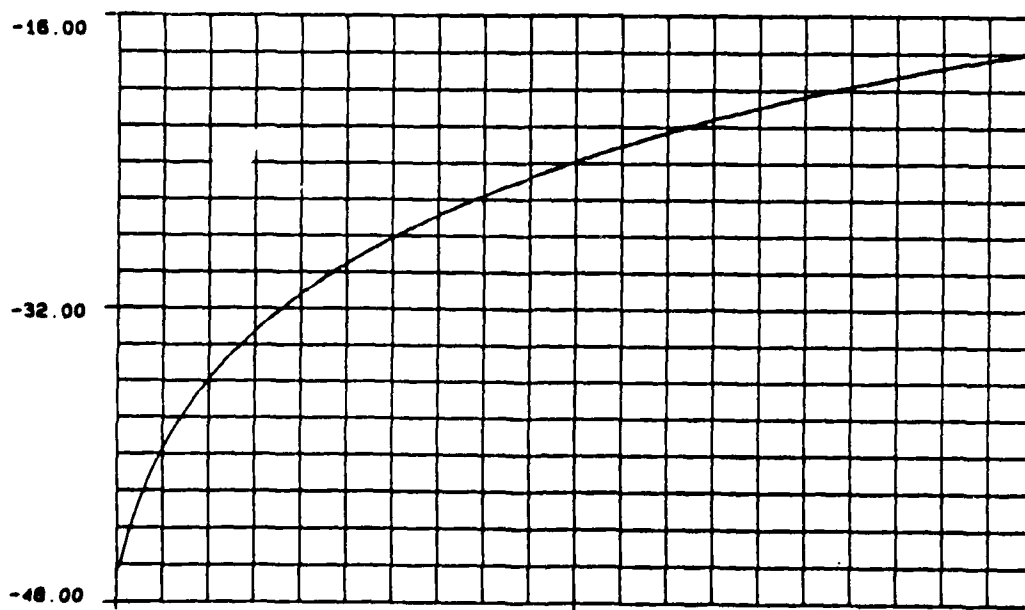


Figure 55. HP 8510 ANA measured coupling.

If it is assumed that a 320 ps rise time represents 1/4 of a sinusoid, then the frequency of the sinusoid will be approximately  $1/(4 \times 320 \text{ ps}) = 780 \text{ MHz}$ . According to the frequency domain data of Fig. 55, the coupling due to a 780 MHz signal is about -16 dB. To test this assumption, the coupling caused by the clock signal of Fig. 56 was measured. The resulting coupling is shown in Fig. 57. An HP 8080A pulse generator was used as the signal source and the HP 54110D digital oscilloscope captured the response. The input signal was 1.152V peak-to-peak with 320 ps rise times - the same as the assumption above. The cross talk of Fig. 57 has a 0.165V peak-to-peak level, equating to -16.8 dB coupling and in agreement with the measured frequency domain data. The measurements of coupling indicate that a 100 MHz clock signal with transition times of 320 ps or greater will generate a measurable but acceptable level of coupling on an adjacent signal line. Clock signals with 1 ns or greater transition times will generate negligible cross talk to adjacent signal lines.

#### 4.8.7 R-L-C Circuit Model

To convert from the TOUCHSTONE distributed model to a circuit model, the element values for the R-L-C prototypes of each transmission line section were determined. Since the distributed model was in agreement with the measured data, it was used as a starting point for calculating the R-L-C values. Fig. 58 shows three sections of the package and their associated prototype circuits.

The final model will be as shown in Fig. 59. It consists of 5 main sections:

1. The package lead (ribbon)
2. The piece of lead brazed to the top layer (microstrip)
3. The internal signal line (stripline)
4. The bond pads (microstrip)
5. The coupling capacitors connecting adjacent signal lines.

The following numbers and calculations are for the longest (worst case) signal lines. Assuming a 200 mil length for the package lead, the series inductance is approximately 4 nH (from a table of ribbon inductance versus length for various widths of ribbon). Approximately 2 ohms was measured for the DC resistance of the package (from lead to opposite lead of test fixture). The resistance values of all the sections of the package will be lumped into a single resistor ( $R_0$ ) for the model.

To convert the transmission line sections into inductors and capacitors the following equations will be used.

$$C = \text{capacitance/length} = 1/v_p Z_0$$

$$L = \text{inductance/length} = Z_0/v_p$$



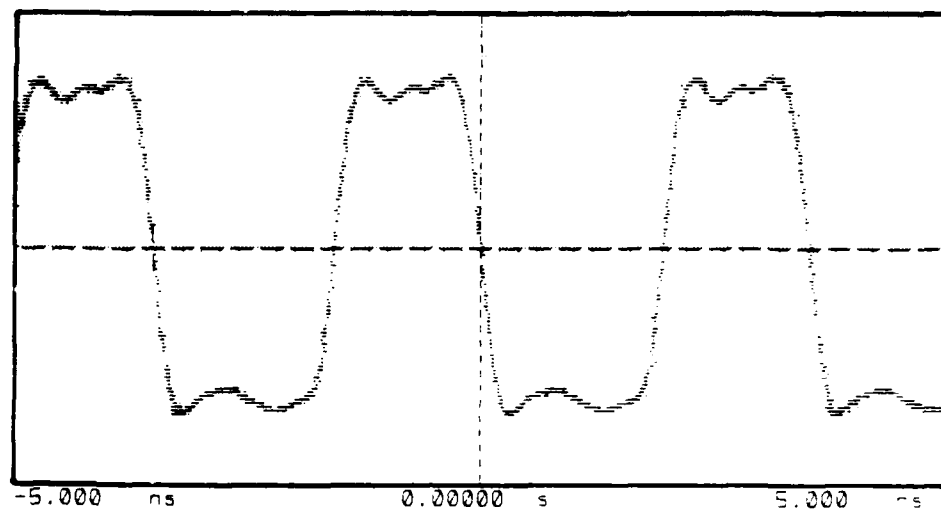


Figure 56. Coupling test signal, 300 ps rise time, 320 ps fall time.

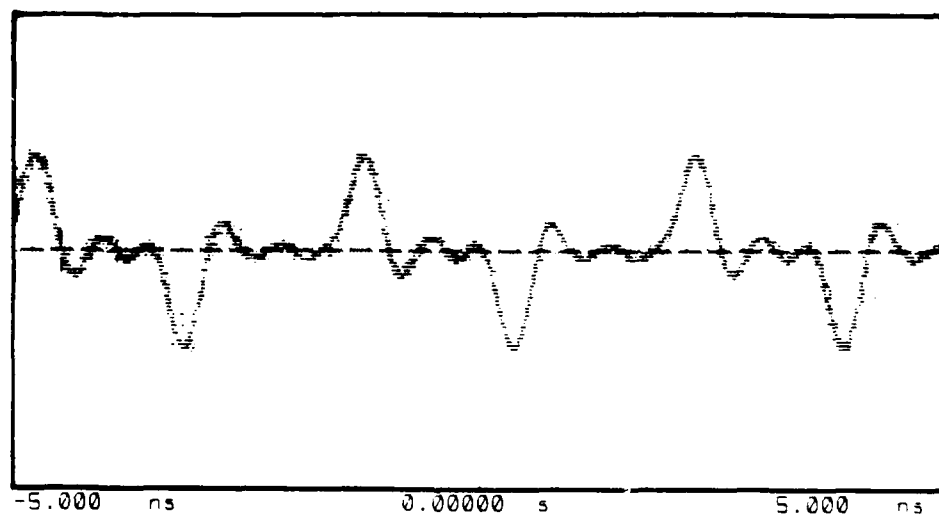


Figure 57. Measured coupling caused by signal of -16.8 dB down from input signal.

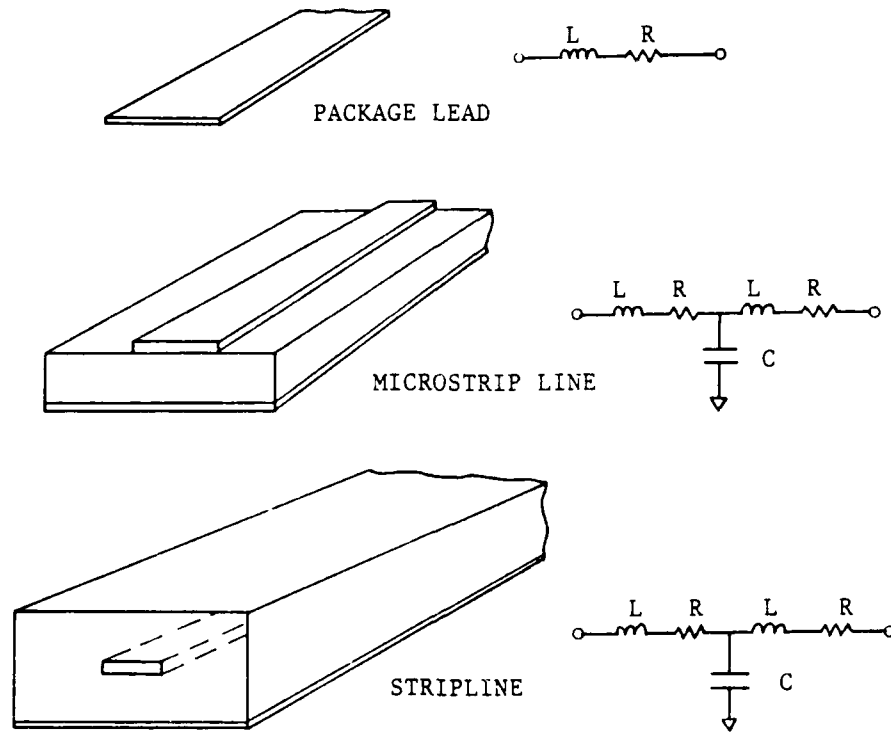


Figure 58. Transmission lines and their associated prototype circuits.

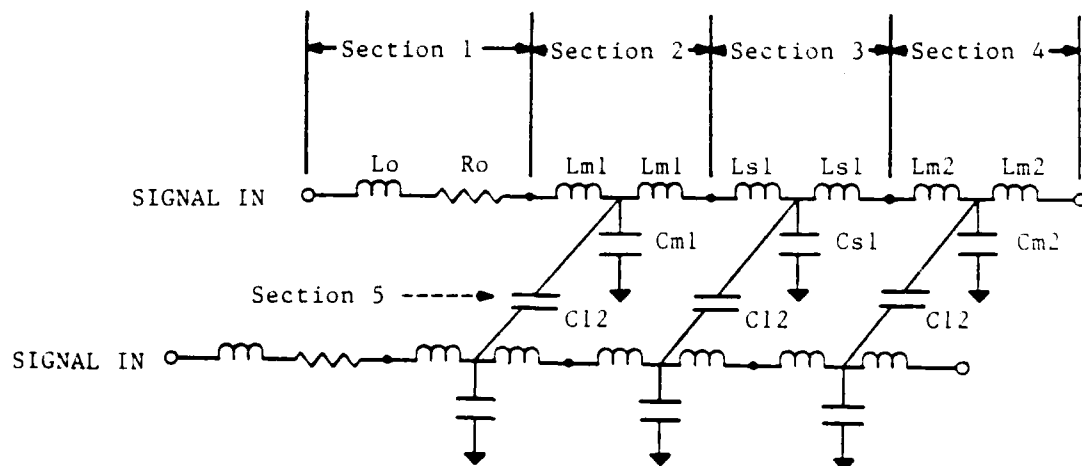


Figure 59. Final model form for two coupled signal lines.

The velocity of propagation of the signals will be:

$$v_p = c/\text{SQRT}(E_r)$$

where  $c = 3 \times 10^8$  m/s

$E_r = 9.6$  for  $\text{Al}_2\text{O}_3$

$$v_p = 0.96824 \times 10^8 \text{ m/s} = 3.81199 \times 10^{12} \text{ mil/s}$$

$Z_0$  = characteristic impedance

The characteristic impedance ( $Z_0$ ) for the first microstrip line (Fig. 42, Section 2) is determined from a "Wheeler Curve" for microstrip. An example of such a curve is given in Fig. 60. The curve gives the characteristic impedance of a line versus the  $w/h$  ratio, for various dielectric materials ( $E_r$ ).

MICROSTRIP CHARACTERIZATION IMPEDANCE CALCULATED FROM WORK OF WHEELER

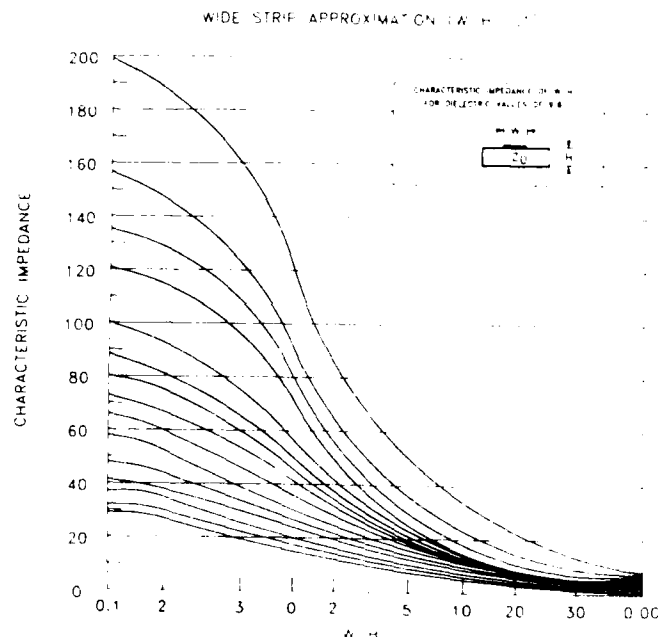


Figure 60. "WHEELER CURVE" for microstrip lines.

For the 196 lead LABCOM package:

Section 1, microstrip

$w$  = strip width = 20 mil

$h$  = dielectric thickness = 7 mil

$l$  = length of line = 30 mil, and  $w/h = 2.85$

$E_r = 9.6$ , therefore from Fig. 60,  $Z_0 = 28$  ohms.

Now,  $C = 1/v_r Z_0 = 9.368 \times 10^{-15} \text{ F/mil}$

$$L = Z_0/v_r = 7.345 \times 10^{-12} \text{ H/mil}$$

For the model, this value is divided into two elements; so,

$$L/2 = 3.672 \times 10^{-12} \text{ H/mil}.$$

With  $l = 30 \text{ mil}$  we have,  $C_{m1} = 0.281 \text{ pF}$   
and  $L_{m1} = 0.110 \text{ nH}$ .

The characteristic impedance for the second microstrip line (Fig. 42, Section 4) is found from,

$$w = 8 \text{ mil}$$

$$h = 7 \text{ mil}$$

$$l = 25 \text{ mil}, \text{ and } w/h = 1.142.$$

From the curve for  $E_r = 9.6$ , we have  $Z_0 = 48 \text{ ohm}$

$$\text{and } C = 1/v_r Z_0 = 5.465 \times 10^{-15} \text{ F/mil}$$

$$L = Z_0/v_r = 12.591 \times 10^{-12} \text{ H/mil}$$

$$\text{and, } L/2 = 6.295 \times 10^{-12} \text{ H/mil}.$$

With  $l = 25 \text{ mil}$ , we have  $C_{m2} = 0.136 \text{ pf}$ , and  $L_{m2} = 0.157 \text{ nH}$ .

The characteristic impedance of the stripline section (Fig. 42, Section 3) is determined from another "Wheeler Curve", Fig. 61. With

$$w = \text{strip width} = 8 \text{ mil}$$

$$b = \text{dielectric thickness} = 14 \text{ mil}, w/b = .571$$

$$t = \text{conductor thickness} = 0, t/b = 0$$

$$l = \text{length of line} = 150 \text{ mil}.$$

Now

$$C = 1/v_r Z_0 = 8.744 \times 10^{-15} \text{ F/mil}$$

$$L = Z_0/v_r = 7.869 \times 10^{-12} \text{ H/mil}$$

$$L/2 = 3.934 \times 10^{-12} \text{ H/mil}.$$

For a 150 mil stripline,  $C_{s1} = 1.316 \text{ pF}$   
 $L_{s1} = 0.600 \text{ nH}$ .

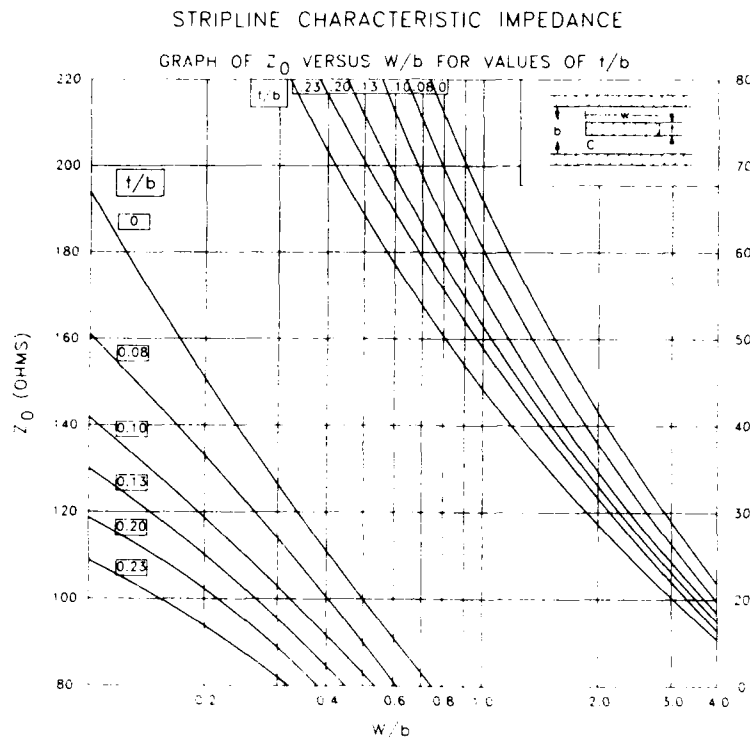


Figure 61. "WHEELER CURVE" for striplines.

To determine the coupling capacitance ( $C_{12}$ ) between adjacent signal lines, the even- and odd-mode impedances of the coupling network was determined. Using custom analysis software, the impedances of each coupled line was determined to be:

$$Z_{oe} = \text{even-mode impedance} = 32.5 \text{ ohm}$$

$$Z_{oo} = \text{odd-mode impedance} = 27.6 \text{ ohm.}$$

The coupling mode impedance ( $Z_{12}$ ) is given by:

$$Z_{12} = 2 / ((1/Z_{oo}) - (1/Z_{oe})) = 266 \text{ ohm.}$$

The even- and odd-mode impedances determined by the analysis software agree with the  $Z_0$  determined from the stripline curve.

$$C = 1/v_r Z_{12} = 0.716 \times 10^{-15} \text{ F/mil}$$

Since the signal lines traverse 150 mil parallel, it was determined that

$$C_{12} = \text{coupling capacitance} = 0.107 \text{ pF.}$$

Fig. 62 shows the TOUCHSTONE model with the calculated R-L-C values. The model (S11 and S21) frequency response data are given in Fig. 63 and Fig. 64 respectively. The S11 results agree with the measured data (Fig. 56). The S21 results for the R-L-C TOUCHSTONE model are slightly rounded compared to the measured data. However, the S21 results accurately model the actual package response. Both measured and modeled S21 data have approximately 0.6 to 0.7 dB insertion loss over the gigahertz bandwidth of the plots. The R-L-C values of Fig. 62 effectively model the reflection and transmission characteristics of the package.

```

DIM
  FREQ MHZ
  RES OH
  IND NH
  CAP PF
  LNG MIL
CKT
  ILABCOM PACKAGE INTERNAL WALL NETWORK *** **
    IND 10 20 L=4.0
    RES 20 30 R=.5
    IND 30 40 L=.110
    CAP 40 00 C=.281
    IND 40 60 L=.110
    IND 60 70 L=.600
    CAP 70 00 C=1.316
    IND 70 90 L=.600
    IND 90 92 L=.157
    CAP 92 00 C=.136
    IND 92 94 L=.157
    DEF2P 10 94 RLC1IN
  ITRANSMISSION LINE MOUNTED INSIDE PACKAGE *** **
    WIRE 100 110 D=.5 L=.75 RHO=1
    MSUB ER=9.6 H=.15 T=.5 RHO=1 RGH=0
    MLIN 110 120 W=.15 L=1075
    WIRE 120 130 D=.5 L=.75 RHO=1
    DEF2P 100 130 MIDLINE
  ITRANSMISSION LINE MOUNTED OUTSIDE PACKAGE *** **
    MSUB ER=9.6 H=.15 T=.5 RHO=1 RGH=0
    MLIN 150 160 W=.15 L=363
    DEF2P 150 160 START
  ILABCOM PACKAGE INTERNAL WALL MODEL (REVERSED) *** **
    IND 200 210 L=.157
    CAP 210 000 C=.136
    IND 210 230 L=.157
    IND 230 240 L=.600
    CAP 240 000 C=1.316
    IND 240 260 L=.600
    IND 260 270 L=.110
    CAP 270 000 C=.281
    IND 270 272 L=.110
    RES 272 274 R=.5
    IND 274 280 L=4.0
    DEF2P 200 280 RLC1OUT
  I R-L-C ELEMENT MODEL OF PACKAGE AND TEST FIXTURE (IDEAL CASE)**
    START 1 2
    RLC1IN 2 3
    MIDLINE 3 4
    RLC1OUT 4 5
    START 5 6
  DEF2P 1 6 RLC1PKG
  OUT
    RLC1PKG DB(S21) GR2
    RLC1PKG DB(S11) GR3
  FREQ
    SWEEP 50 1250 20

```

} Test  
} Fixture

Figure 62. Final TOUCHSTONE R-L-C model.

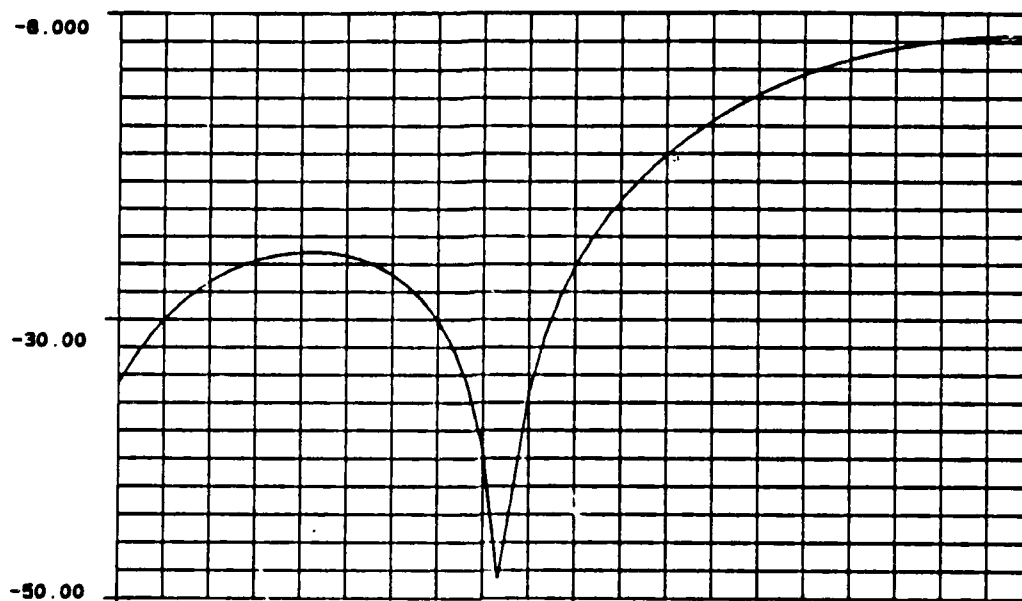


Figure 63. Final TOUCHSTONE R-L-C model (S11) results.

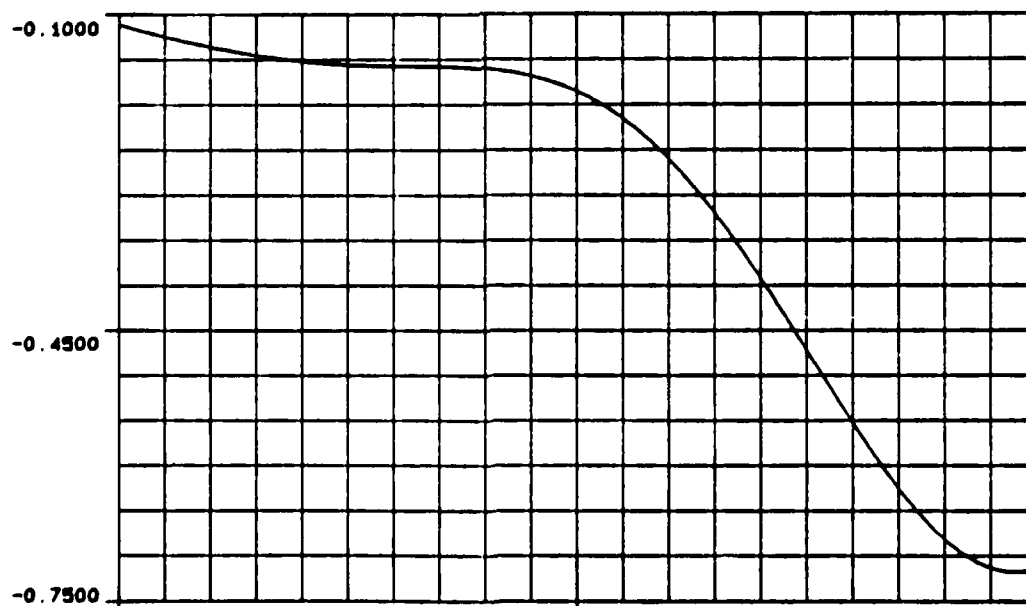


Figure 64. Final TOUCHSTONE R-L-C model (S21) results.

The calculated coupling capacitance (C12) was included in the TOUCHSTONE model in three locations (Fig. 59). The calculated value predicted less coupling than was measured. Therefore, the capacitance was increased to provide results comparable to the measured data. The data for S11 and S21 given in Figs. 63 and 64 were verified for the case where the coupling capacitors are included in the model. Fig. 65 shows the modeled coupling response (C12 = 0.3 pF). As expected, the coupling response is exponentially increasing with frequency and in agreement with the measured data of Fig. 55.

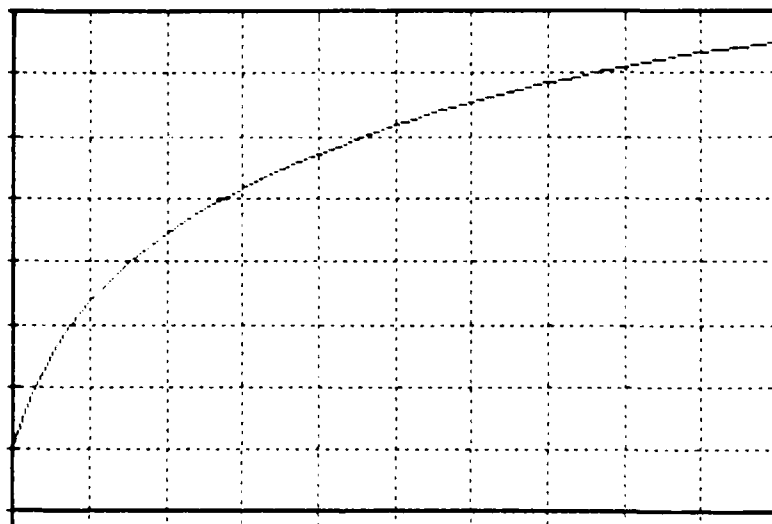


Figure 65. TOUCHSTONE model coupling results.

The complete R-L-C model for the LABCOM VHSIC 196-lead multichip package is shown in Fig. 66 along with the final element values. The measured data in this report is for 50 ohm load conditions and loads other than 50 ohms will have different responses. The model however, is valid for any load conditions.



$L_{m1}$	= .110 nH	$C_{12}$	= .300 pF
$C_{m1}$	= .281 pF	$R_o$	= .500 ohm
$L_{s1}$	= .600 nH	$L_o$	= 4.000 nH
$C_{s1}$	= 1.316 pF		
$L_{m2}$	= .157 nH		
$C_{m2}$	= .136 pF		

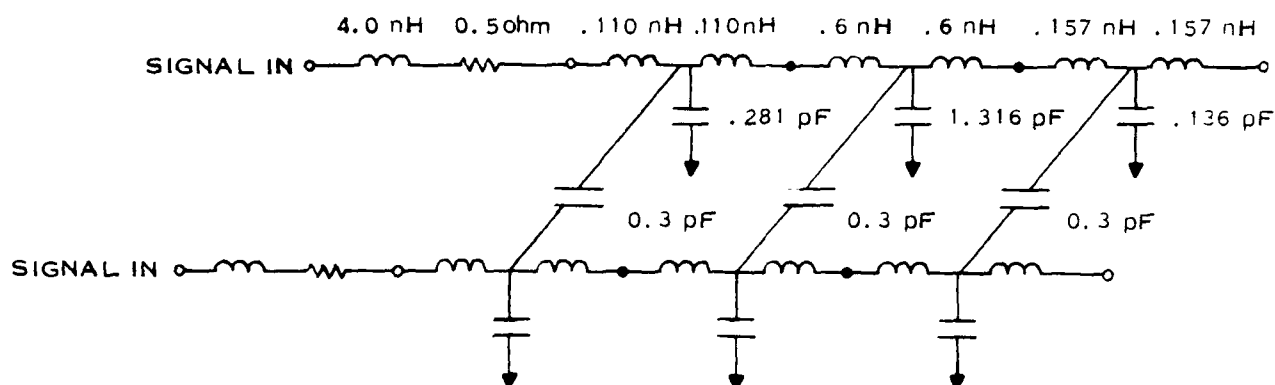


Figure 66. Final R-L-C model for the LABCOM (VHSIC) multichip package.

#### 4.8.8 Conclusions and Comments

As shown in Fig. 38, the lower ground plane has holes in it which provides more dielectric surface area to improve the structural strength of the package. These holes may have an effect on the signal propagation at frequencies above several gigahertz. At frequencies below 1 GHz these holes do not present any problems to signal propagation. The parallel ground planes were included in this package to improve the signal propagation over a wide range of frequencies by providing a stable characteristic impedance.

Lead and signal line length are important to the performance of a package. Every inch of path length adds approximately 100-300 ps of delay to the signal. System designers of fast ECL type devices must incorporate these delays into their timing considerations for clock rates above 50-100 MHz. Capacitive coupling increases with path length which increases cross talk and lowers the bandwidth of the package. Line lengths should be kept to a minimum. In the LABCOM 196-lead package the longest path length is approximately 350 mil including a 200 mil lead.

Lower dielectric constants increase the signal propagation velocity which effectively decreases the path length and improves transmission and cross talk properties of the package. The LABCOM multichip package uses  $\text{Al}_2\text{O}_3$  ( $E_r = 9.6$ ) dielectric because of its good hermitic properties. If hermiticity is not a great concern, polyimide substrates ( $E_r = 3.5$ ) may be used to improve package transfer properties. Inorganic chip carrier substrates are being developed that exhibit dielectric constants of 1.5-2.0. Also, fine metal lines of non-refractory metals are being developed to improve package properties. Thinner traces allow wider gaps between signal lines (inhibiting cross talk) but may increase the resistance of the line. The layer thickness should be kept thin in order to confine the signal field lines in the ground planes which will inhibit cross talk to adjacent signals.

In summary, short line length, low dielectric constants, thin layers, narrow signal traces, wide gaps between traces and adequate grounding are all conditions that may improve signal handling properties of a package. To maintain a specific characteristic impedance ( $Z_0$ ), certain dimensional and material criteria must be met. Also, the structural and environmental integrity of the package must be considered when making choices to improve the electrical properties of the package.

The LABCOM 196-lead multichip package developed at TI and fabricated at Interamics performs exceedingly well as a carrier for VHSIC chips. The package is designed as a multichip carrier for VHSIC chips that require signals of 100 MHz and transition times of approximately 1 ns. The measured data given in this report clearly show that the package meets and exceeds the signal handling requirements and provides high I/O count to accommodate multichip use.

#### 4.9 196-PIN PACKAGE POWER AND GROUND PLANE CHARACTERIZATION

The power and ground plane characterization tests were conducted in order to observe and study the electrical behavior of the power and ground systems of the LABCOM VMC 196-pin package. It is important that the package be able to supply the power needs of several VHSIC devices without degrading the quality of the supply voltage.

The Cold Start Power-up Test was conducted to study the natural time delay that the power planes experience when the power to the package is turned on. The power plane over ground plane construction of the package creates a capacitance that will introduce a charge-up time delay. Fig. 67 is a model of the package power plane's equivalent circuit. Using a known resistance to simulate a load, and studying the time constant of the power-up waveform, the inherent capacitance of the power planes can be determined.

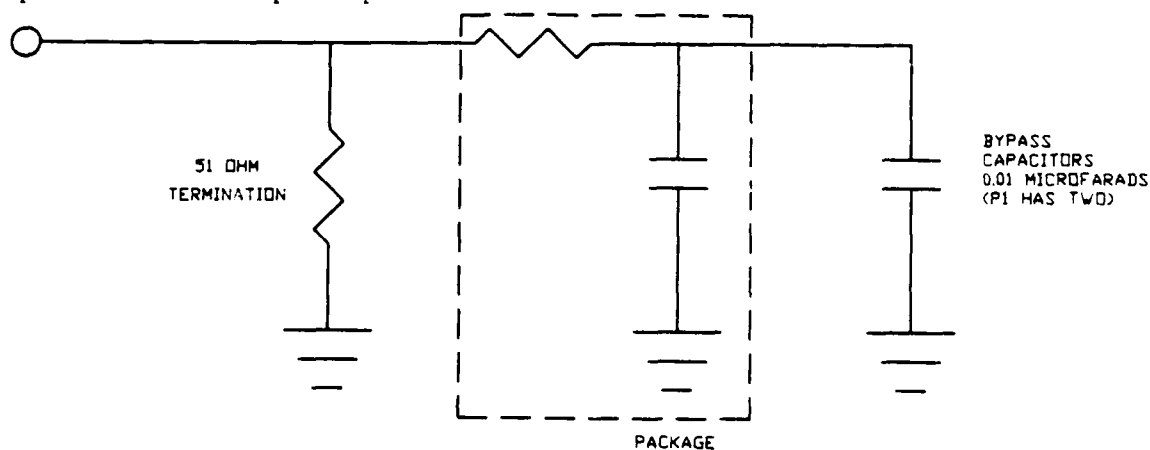


Figure 67. Package equivalent circuit.

Because printed circuit board constraints might prevent a designer from hooking up all of the pins of the power and/or ground planes, the Low Current Voltage Drop test was performed to determine the voltage drops around the planes at a particular current level. A small current is forced into one of the pins of the plane under test and sunk from another pin. The voltage created across the plane is measured and recorded. This process is repeated until all combinations of pins have been tested. To complement this test, the resistance between each combination of pins is measured and recorded.

The Infrared Analysis was conducted to determine which structures of the power planes are subject to  $I^2R$  heating under a high-current load. A relatively large current is forced into the pins and a thermal image is made using the UTI 9000 Computerized Color Thermograph. These thermal images are photographed from the thermograph and are included in this report.

The purpose of the Maximum Current Delivery Test is to determine how much current the package's power system is able to withstand. The current through the package is steadily increased until one of the power system structures is destroyed. This value of current is measured and recorded.

#### 4.9.1 Cold Start Power-up Test

##### Tests Without the Package

The following tests were performed in order to observe the effects of the test equipment and bypass capacitors so that these components could be calibrated out of the final results. By studying the waveforms produced by these tests and comparing them to the waveforms from the tests involving the package, the electrical properties of the power planes were determined.

##### 51-ohm Resistor

The power-up waveform of the 51-ohm resistor only was observed and photographed to study the characteristics of the power supply and relay circuit and to compare the waveform with those of the power planes. A 51-ohm resistor was chosen because it is typically a good termination for a signal line and because it would simulate a 500 mW load to a 5V power supply.

It can be seen from the waveform photographs that the relay in the test circuit exhibits a switch bounce problem (Fig. F-1 of "Cold Start Power-on Test Procedure", Dwg. No. 2437697, in Appendix F).

The 1  $\mu$ s/div waveform shown in Fig. 68 shows that the relay opens up approximately 2.2  $\mu$ s after it initially closes. Almost 3  $\mu$ s later, the relay closes again.



Figure 68. 51-ohm resistor, 1  $\mu$ s/div, 2V/div.

The 20  $\mu\text{s}/\text{div}$  waveform of Fig. 69 shows that the relay needs approximately 80  $\mu\text{s}$  to stabilize in the "switch closed" mode.

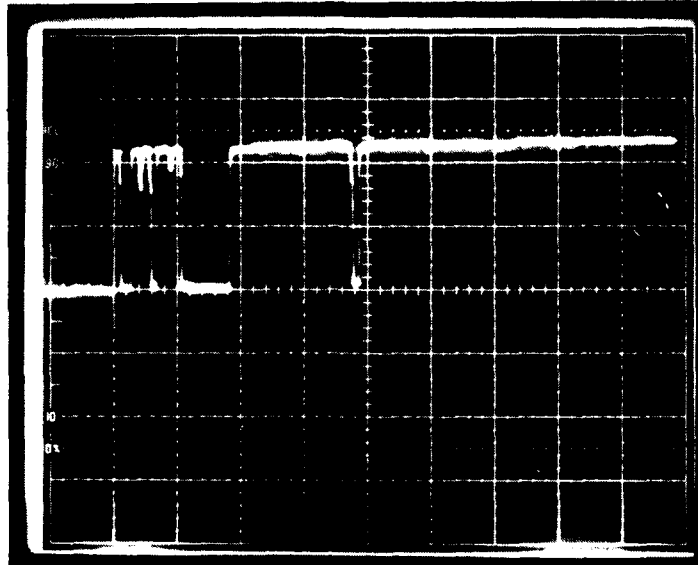


Figure 69. 51-ohm resistor, 20  $\mu\text{s}/\text{div}$ , 2V/div.

Even though the relay switch bounce phenomenon affected the results of this test, we were able to gather some important data about the power plane power-up characteristics. The time intervals between openings and closings of the relay were long enough to charge and discharge the power planes and bypass capacitors of the package and thus we were able to observe the natural time constant of the planes with and without the bypass capacitors.

#### 51-ohm Resistor and Two 0.01 $\mu\text{F}$ Capacitors

The two 0.01  $\mu\text{F}$  capacitors were added for this test to simulate the noise bypass capacitors which would normally be connected to the primary power plane, P1, inside the package. As Fig. 70 shows, this RC network now exhibits the characteristics of overshoot, settling time, and exponential decay.

The overshoot rises to approximately 7.1V. From the equation,

$$\text{P.O.} = \frac{7.1 - 5}{5} \star 100\% \quad (1)$$

the percent overshoot is found to be 42%. It is difficult to find a settling time for the network because the relay bounces open before the system can settle. The opening of the relay creates a charged, unexcited RC network which immediately begins to decay. From the equation

$$v(t) = V e^{-t/RC} \quad (2)$$

we know that the voltage signal should decay to  $5e^{-1}$  or 1.84 volts after one time constant. From Fig. 70, it can be seen that the voltage decays to 1.8V after approximately 1  $\mu$ s. This time then is the time constant of the circuit. Checking mathematically, the time constant ( $t$ ) of the circuit should be:

$$t = RC = (51 \text{ ohm})(0.02 \text{ } \mu\text{F}) = 1.02 \text{ } \mu\text{s} \quad (3)$$

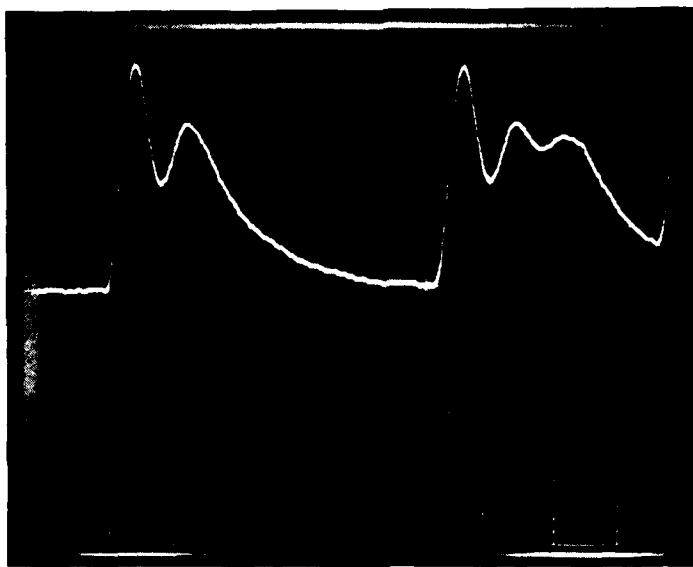


Figure 70. 51-ohm resistor and two 0.01  $\mu$ F capacitors, 1  $\mu$ s/div, 2V/div.

51-ohm Resistor and One 0.01  $\mu$ F Capacitor

This test is the same as that described above except that only one 0.01  $\mu$ F capacitor was used to simulate the single bypass capacitors on the secondary (P2) and tertiary (P3) power planes. The overshoot in this case is

$$\text{P.O.} = \frac{6.8 - 5}{5} * 100\% = 36\% \quad (4)$$

It is difficult to find the settling time for this case also due to the bouncing of the relay. The time constant for this case was found from Fig. 71 and equation 2 to be approximately 0.7  $\mu$ s. Checking mathematically, the time constant ( $t$ ) of the circuit should be

$$t = RC = (51 \text{ ohm})(0.01 \text{ } \mu\text{F}) = 0.51 \text{ } \mu\text{s} \quad (5)$$

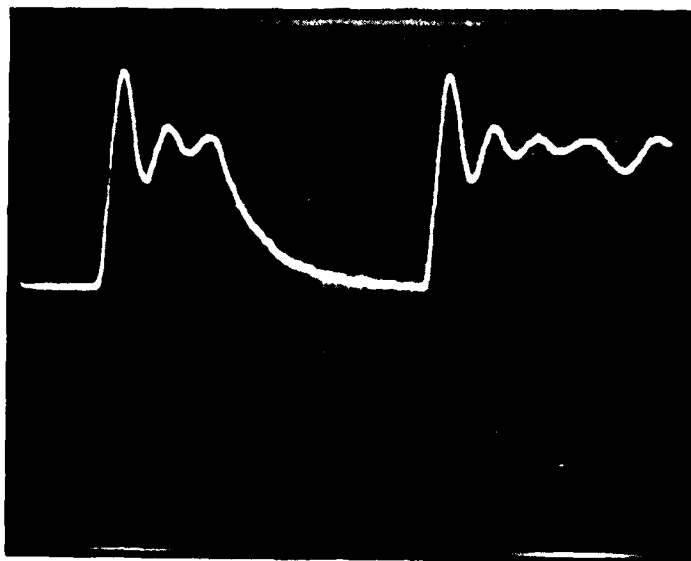


Figure 71. 51-ohm resistor and 0.01  $\mu$ F capacitor, 1  $\mu$ s/div, 2V/div.

#### 4.9.2 Package Power Plane Tests

##### Primary Power Plane With 51-ohm Termination

Comparison of the power-up waveform of the primary power plane (Fig. 72) with that of the 51-ohm resistor alone (Fig. 68) reveals an important fact. The power plane causes very little change in the waveform. Close examination of Fig. 72 shows that the inherent capacitance of the power plane does introduce a small overshoot spike which is quickly damped. Also, the voltage signal has time to settle before the relay bounces open. The power plane capacitance causes the signal to fall more slowly after the relay opens, but the difference in time is only about 0.1  $\mu$ s.

##### Primary Power Plane With 51-ohm Termination and Two 0.01 $\mu$ F Capacitors

Two 0.01  $\mu$ F chip capacitors were installed in the bypass capacitor pads of the primary power plane. The resulting power-up waveform is shown in Fig. 73. The bypass capacitors caused a dramatic increase in the overshoot, settling time, and decay time constant when compared with the results of the power plane with no capacitors. However, comparison with Fig. 70 (51-ohm resistor and 0.02  $\mu$ F capacitance only) shows that the package capacitance is very small compared to that of the bypass capacitors. The percent overshoot for this case is

$$\text{P.O.} = \frac{6.6 - 5}{5} * 100\% = 32\% \quad (6)$$

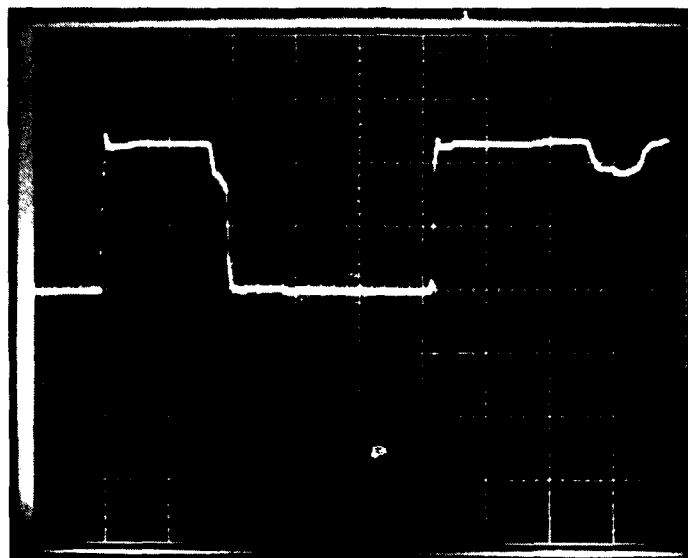


Figure 72. Primary power plane with 51-ohm termination, 1  $\mu$ s/div, 2V/div.



Figure 73. Primary power plane with 51-ohm termination and two 0.01  $\mu$ F capacitors, 1  $\mu$ s/div, 2V/div.



The decay time constant ( $t$ ) was found from Figure 73 and equation 2 to be approximately  $1.1 \mu\text{s}$ . If  $R$  is assumed to be  $51 \text{ ohms}$ , then the total capacitance can be found to be

$$C = t/R = 1.1 \mu\text{s}/51 \text{ ohms} = 0.0216 \mu\text{F} \quad (7)$$

The capacitance of the primary power plane must then be approximately  $0.0016 \mu\text{F}$ .

#### Secondary Power Plane With 51-ohm Termination

As was the case with the primary power plane with only a resistive termination (Fig. 72), the secondary power plane power-up characteristic is only slightly different than that of the  $51\text{-ohm}$  resistor alone (Fig. 68). The secondary power plane did not produce much of an overshoot at all and the voltage settles out rapidly. Fig. 74 shows that the voltage decay that occurs after the relay opens up is very rapid, but the decay is slightly slower for this case than for the primary power plane. The difference is too small, however, to measure accurately from the photographs.

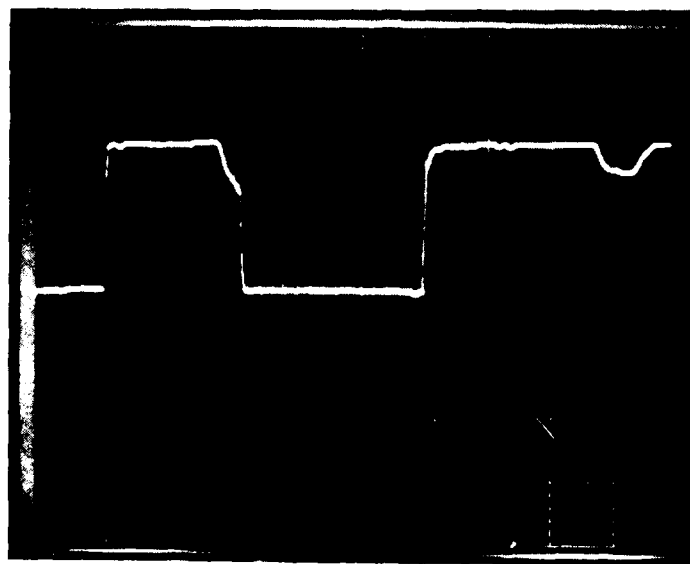


Figure 74. Secondary power plane with 51-ohm termination  $1 \mu\text{s}/\text{div}$ ,  $2\text{V}/\text{div}$ .

### Secondary Power Plane With 51-ohm Termination and 0.01 $\mu$ F Bypass Capacitors

A 0.01  $\mu$ F chip capacitor was installed in the bypass capacitor pad of the secondary power plane. The resulting power-up waveform is shown in Fig. 75. The bypass capacitor caused the overshoot, settling time, and decay time constant to increase significantly compared to the power plane with no capacitors. A comparison with the waveform of the resistor and capacitor alone (Fig. 71), however, shows that the capacitance of the power plane must be small compared to that of the bypass capacitors. The percent overshoot for this case is

$$P.O. = \frac{6.4 - 5}{5} * 100\% = 28\% \quad (8)$$

The decay time constant ( $t$ ) was found from Fig. 75 and equation 2 to be approximately 0.6  $\mu$ sec. If  $R$  is assumed to be 51 ohms, then the total capacitance can be found to be

$$C = t/R = 0.6 \mu s / 51 \text{ ohms} = 0.0118 \mu F \quad (9)$$

The capacitance of the primary power plane must then be approximately 0.0018  $\mu$ F.

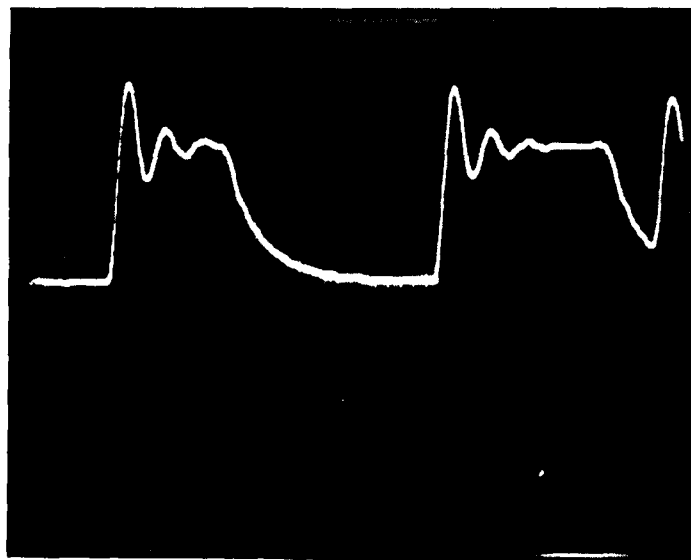


Figure 75. Secondary power plane with 51-ohm termination and 0.01  $\mu$ F capacitor, 1  $\mu$ s/div, 2V/div.

### Tertiary Power Plane With 51-ohm Termination

As was the case with the primary and secondary power planes with only a resistive termination (Figs. 72 and 74 respectively), the tertiary power plane power-up characteristic is only slightly different than that of the 51-ohm resistor alone (Fig. 68). The tertiary power plane produced a very small amount of overshoot and the voltage signal settles out rapidly. Fig. 76 shows that the voltage decay that occurs after the relay opens up is very rapid, but the decay is slightly slower for this case than for the primary and secondary power planes. The difference is too small, however, to measure accurately from the photographs.

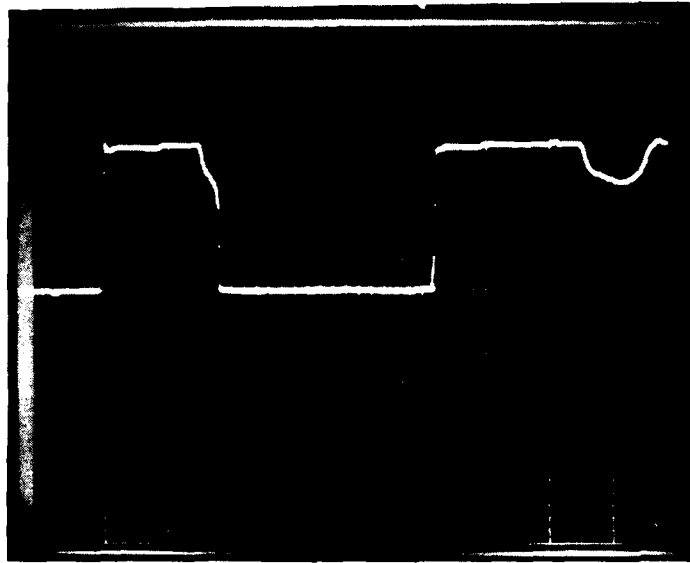


Figure 76. Tertiary power plane with 51-ohm termination 1  $\mu$ s/div, 2V/div.

### Tertiary Power Plane With 51-ohm Termination and 0.01 $\mu$ F Bypass Capacitor

A 0.01  $\mu$ F chip capacitor was installed in the bypass capacitor pad of the tertiary power plane. The resulting power-up waveform is shown in Fig. 77. The bypass capacitor caused the overshoot, settling time, and decay time constant to increase significantly compared to the power plane with no capacitors. A comparison with the waveform of the resistor and capacitor alone (Fig. 71), however, shows that the capacitance of the power plane must be small compared to that of the bypass capacitors. The percent overshoot for this case is

$$P.O. = \frac{6.2 - 5}{5} * 100\% = 24\% \quad (10)$$

The decay time constant ( $t$ ) was found from Fig. 77 and equation 2 to be approximately 0.7  $\mu$ s. If  $R$  is assumed to be 51 ohms, then the total capacitance can be found to be

$$C = t/R = 0.7 \mu\text{s}/51 \text{ ohms} = 0.0378 \mu\text{F} \quad (11)$$

The capacitance of the primary power plane must then be approximately 0.0037  $\mu\text{F}$ .

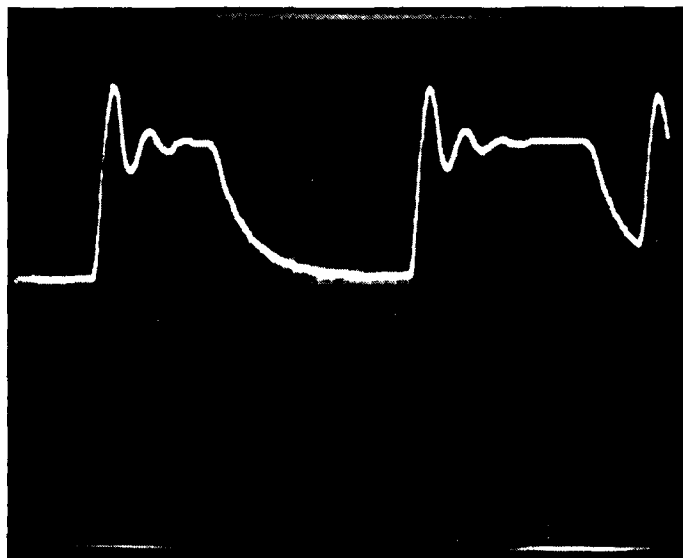


Figure 77. Tertiary power plane with 51-ohm termination and 0.01  $\mu\text{F}$  capacitor, 1  $\mu\text{s}/\text{div}$ , 2V/div.

#### 4.9.3 Low-Current Voltage Drop Test

##### Voltage Drop Measurements

The voltage drop test was conducted by flowing current into a particular pin of the power or ground system under test and sinking that current from another pin of that system. This was done for all combinations of pins on each plane using the power plane test fixture switching scheme. In all tests, the current was regulated with the voltage and current controls of the power supply to be 100 mA  $\pm$  1 mA. The voltage created by the current flow was measured from the package lead braze pad of the pin where the current was supplied to the braze pad of the pin where the current was sunk. The results of this test are presented in Table 11.

From the data gathered in this experiment, it can be seen that voltage drops between pins on opposite sides of the power planes were greater than those between pins on adjacent sides. The data also show that the voltage drops around the secondary power plane are smaller than for the primary power plane. The voltage drops of the secondary plane are smaller because that plane has fewer openings for vias from other networks and thus more conductive

Table 11. 196-pin Package Voltage Drop Measurements.

	<u>Source Pin</u>	<u>Sink Pin</u>	<u>Voltage Drop (mV)</u>
Primary Power Plane, P1	25	74	17.68
	25	123	21.85
	25	172	17.68
	74	123	17.98
	74	172	21.77
	123	172	17.60
Secondary Power Plane, P2	17	66	17.39
	17	115	20.85
	17	164	16.58
	66	115	16.95
	66	164	20.61
	115	164	17.25
Tertiary Power Plane, P3	33	82	19.74
	33	131	24.41
	33	180	20.20
	82	131	19.73
	82	180	24.18
	131	180	19.72
Ground Network	9	41	4.24
	9	58	4.22
	9	90	4.30
	9	107	4.17
	9	139	4.11
	9	156	4.21
	9	188	3.85
	41	58	3.80
	41	90	4.20
	41	107	4.15
	41	139	4.23
	41	156	4.30
	41	188	4.24
	58	90	4.01
	58	107	4.00
	58	139	4.07
	58	156	4.19
	58	188	4.20
	90	107	3.64
	90	139	3.99
	90	156	4.18
	90	188	4.25
	107	139	3.75
	107	156	3.97
	107	188	4.11
	139	156	3.55
	139	188	4.04
	156	188	4.05

material. Although the tertiary power plane has even more conductive material than the secondary plane, the voltage drops are higher for the tertiary plane than for both of the other planes. The advantages gained by having more conductor are lost by having longer vias between the pins and the power plane. The voltage drops around the ground network are relatively small because all of the pins are connected to the base, which has very little resistance.

#### Resistance Measurements

To complement the data gathered from the Low Current Voltage Drop Test and to aid in creating a model of the power and ground systems. The resistances between all combinations of pins of the power and ground systems were measured and are tabulated in Table 12. These measurements were taken from the braze pad of the first pin to the braze pad of the second using a Hewlett-Packard 3478A Multimeter in the two-probe resistance mode. The resistance of the test leads was measured and subtracted from the actual meter reading to produce the results in Table 12.

The data gathered during this test correlates very well with the data gathered during the voltage drop test. The resistances are smaller for the secondary power plane than for the primary due to more conductive material on the secondary plane. The tertiary plane has even more conductive material than the secondary, but the tertiary plane's resistances are higher due to the longer vias from the braze pads to the power plane. The ground plane resistances are very low because all of the pins are connected to the base, which has very little resistance.

#### 4.9.4 Infrared Analysis

The photographs taken of the color thermograph display during the infrared analysis show that the package is able to withstand relatively large amounts of current before the package structures become unacceptably hot. It is obvious from the photographs that the package leads tend to be the hottest structures at high current levels. The lead-to-package braze pads and the vias under them tend to be the next hottest structures.

All tests were conducted in a 20°C, still-air ambient environment. One lead from each power plane was subjected to various amounts of current, and the temperature of the lead was allowed to stabilize. The infrared image of the lead under test was photographed and its temperature recorded. Each lead was tested at one, two, and three amperes of current. Figs. 78 through 86 are the photographs taken of the thermograph display during this test. The colors in the photographs represent the relative temperatures of the structures of the package. The white areas are the hottest and it is the temperature of this area that is recorded for each case. Each color in the photographs represents a region of the temperature gradient. The actual temperature of a particular color depends on the °C per color level (0.1°C/L) and mid-color bar temperature settings on the thermograph. On some of the figures, the cross hairs are centered on the hottest area of the package lead and the actual temperature of that area is displayed in the lower right hand corner of the display.

Table 12. 196-pin Package Resistance Measurements.

	<u>From Pin</u>	<u>To Pin</u>	<u>Resistance (ohms)</u>
Primary Power Plane, P1	25	74	0.155
	25	123	0.197
	25	172	0.154
	74	123	0.170
	74	172	0.199
	123	172	0.180
Secondary Power Plane, P2	17	66	0.154
	17	115	0.181
	17	164	0.129
	66	115	0.145
	66	164	0.166
	115	164	0.141
Tertiary Power Plane, P3	33	82	0.161
	33	131	0.213
	33	180	0.163
	82	131	0.171
	82	180	0.215
	131	180	0.163
Ground Network	9	41	0.037
	9	58	0.036
	9	90	0.037
	9	107	0.038
	9	139	0.034
	9	156	0.032
	9	188	0.031
	41	58	0.036
	41	90	0.033
	41	107	0.044
	41	139	0.038
	41	156	0.034
	41	188	0.036
	58	90	0.029
	58	107	0.036
	58	139	0.040
	58	156	0.039
	58	188	0.036
	90	107	0.032
	90	139	0.035
	90	156	0.031
	90	188	0.033
	107	139	0.040
	107	156	0.038
	107	188	0.031
	139	156	0.038
	139	188	0.040
	156	188	0.039

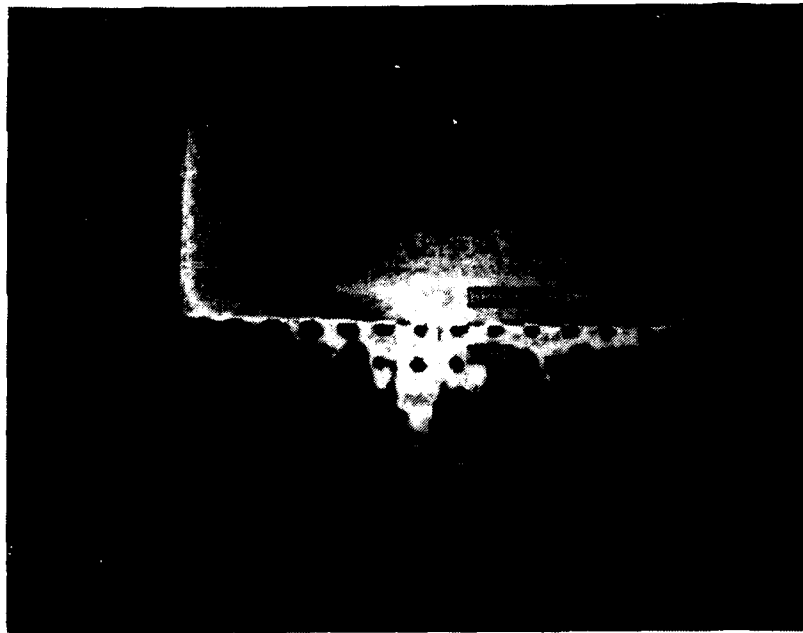


Figure 78. Pin 123 of P1, 1A, maximum temperature 29.8°C.

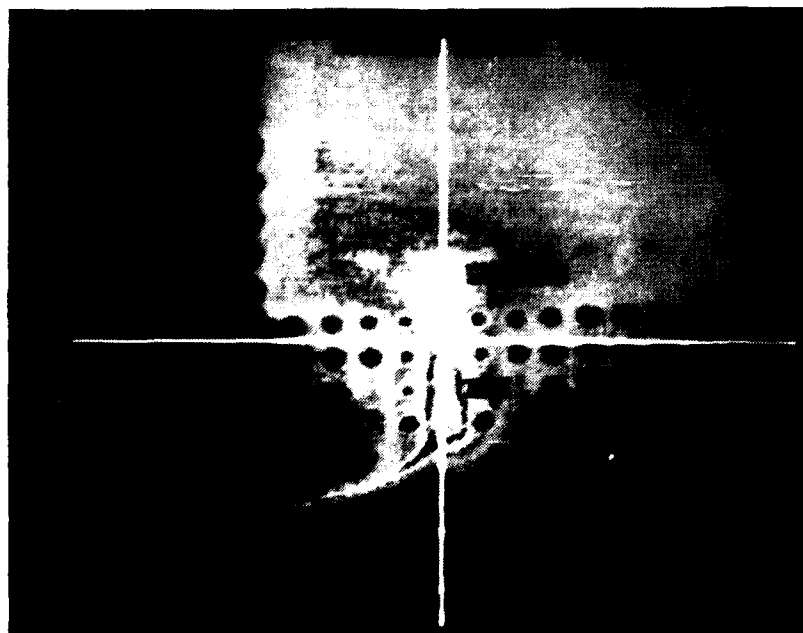


Figure 79. Pin 115 of P2, 1A, maximum temperature 27.2°C.



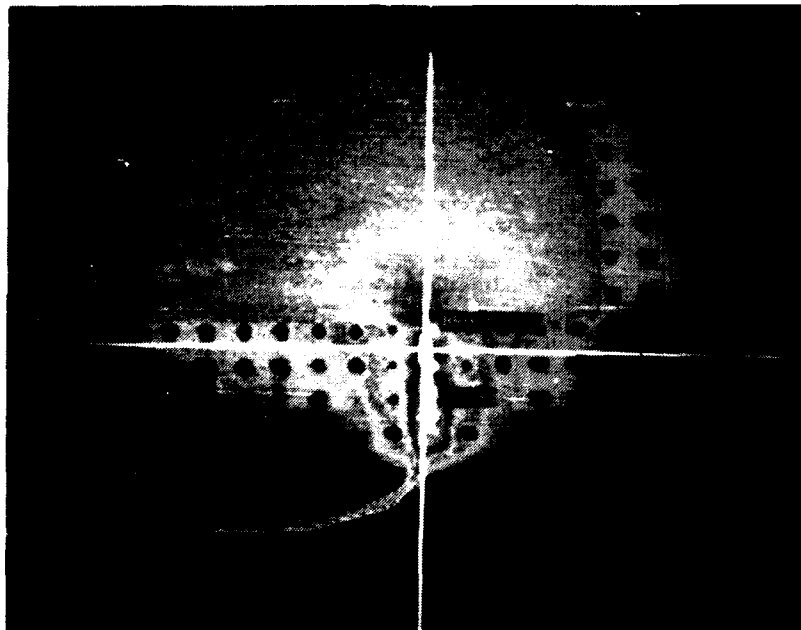


Figure 80. Pin 131 of P3, 1A, maximum temperature 27.2°C.

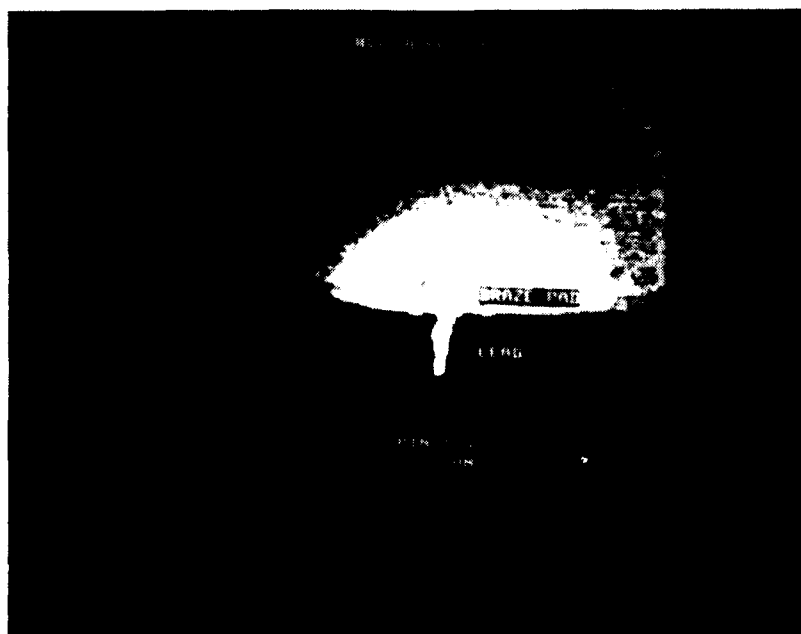


Figure 81. Pin 123 of P1, 2A, maximum temperature 48.2°C.

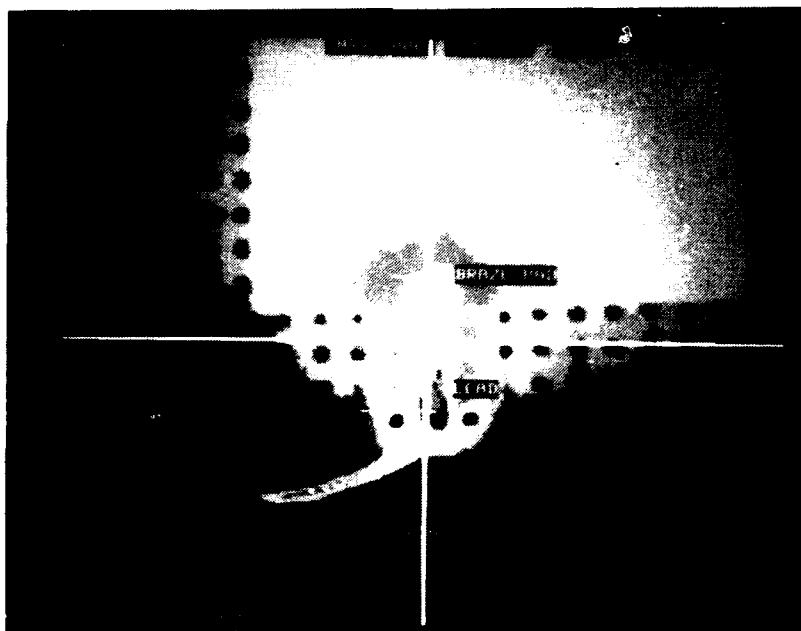


Figure 82. Pin 115 of P2, 2A, maximum temperature 38.4°C.

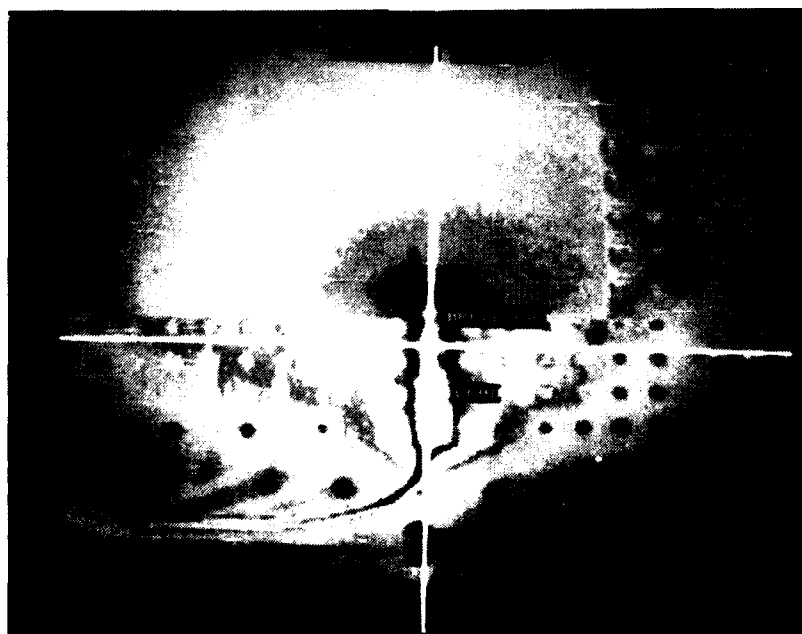


Figure 83. Pin 131 of P3, 2A, maximum temperature 37.6°C.

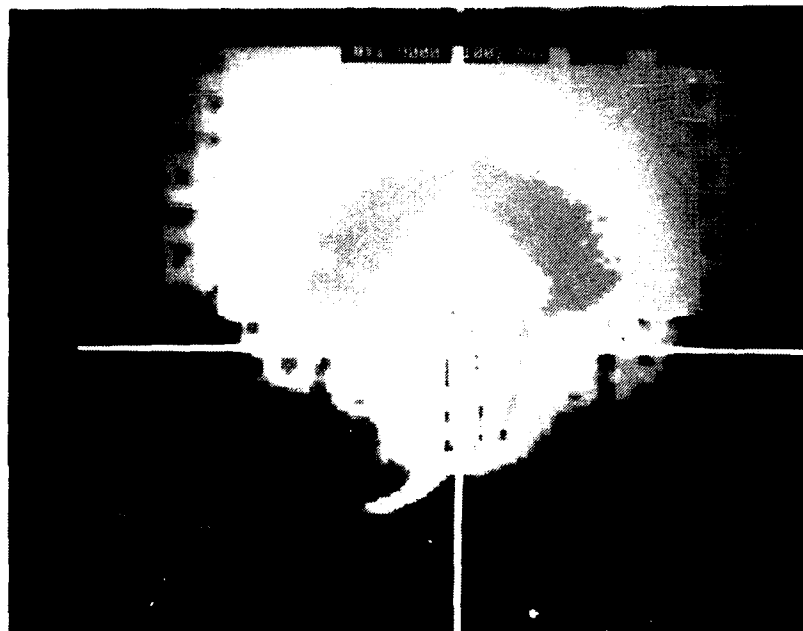


Figure 84. Pin 123 of P1, 3A, maximum temperature 58.5°C.

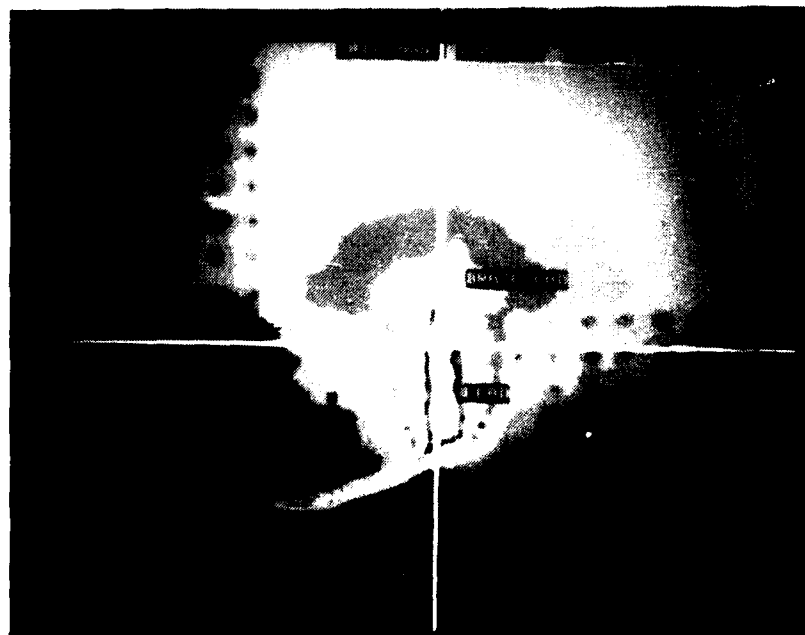


Figure 85. Pin 115 of P2, 3A, maximum temperature 55.7°C.

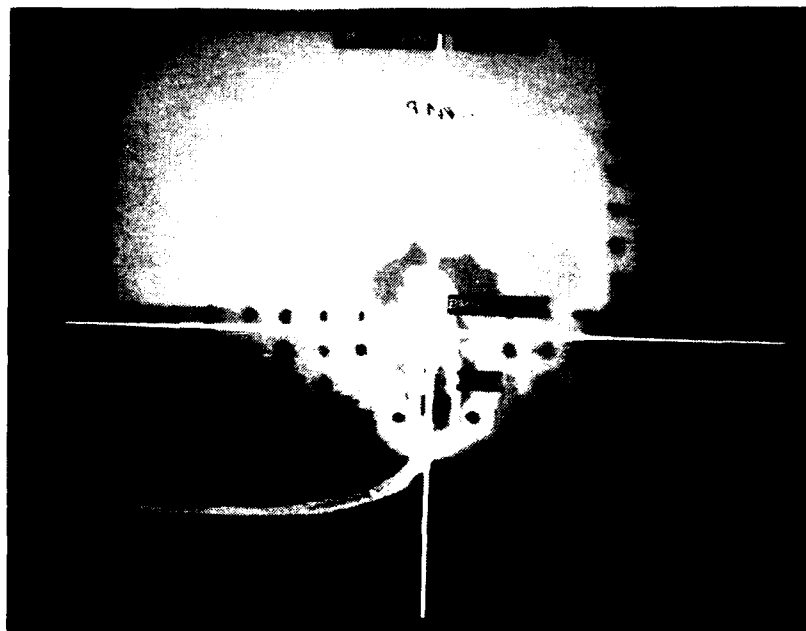


Figure 86. Pin 131 of P3, 3A, maximum temperature 58.0°C.

Additionally, each power plane was photographed with the four leads of the plane carrying a total of 5A of current. Figs. 87 through 89 are the photographs taken of the thermograph display during these tests. As seen in these figures, some of the pins on each plane tend to be slightly hotter than the others. This difference is caused by the wires from the power supply to these leads being somewhat shorter than the others and thus carrying more current due to lower resistance. The actual temperature difference is only a few tenths of a degree Celsius.

#### 4.9.5 Maximum Current Delivery Test

The maximum current carrying capability of the package leads was found by forcing large amounts of current through the leads until they were destroyed. The test started on each lead at approximately 2.5A. The current was slowly increased (0.01 V/s) until the lead was fused and current went to zero. The maximum current for the power and ground leads of a random sample package are given in Table 13. It should be noted that these values are the fuse point of the leads due to an increasing current. It is apparent from the results that the leads cannot be expected to withstand a continuous current of 4A or more. Further tests concluded, however, that the leads can withstand a continuous current of up to 3A.

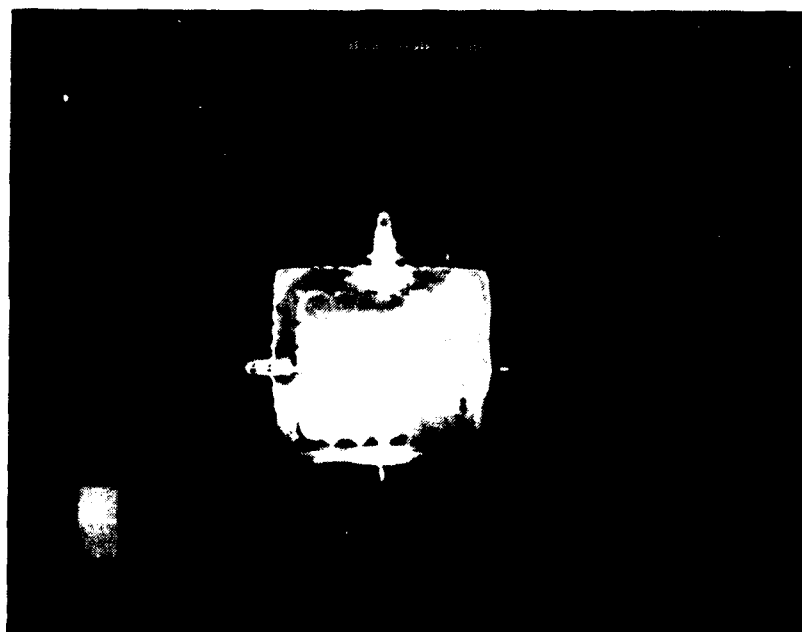


Figure 87. Pins 25, 76, 123 and 172 of P1, 5A total.

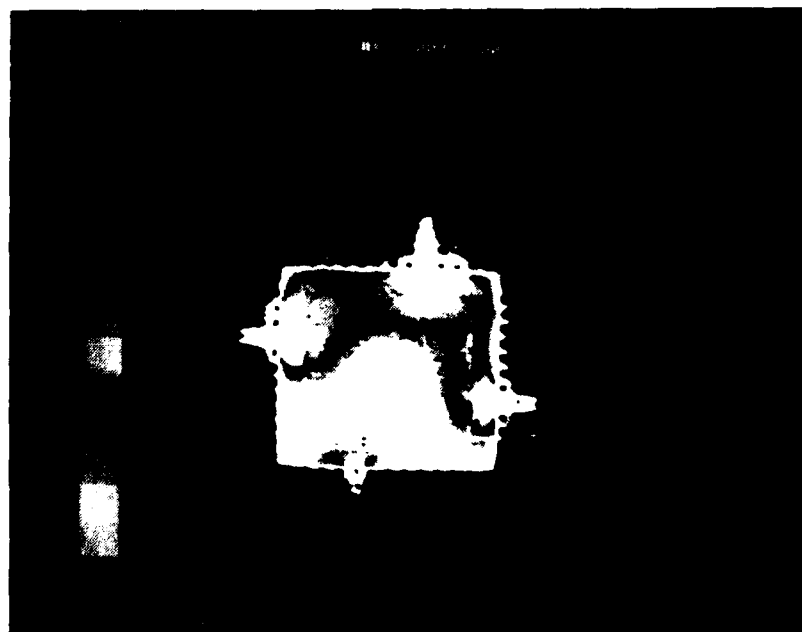


Figure 88. Pins 17, 66, 115 and 164 of P2, 5A total.

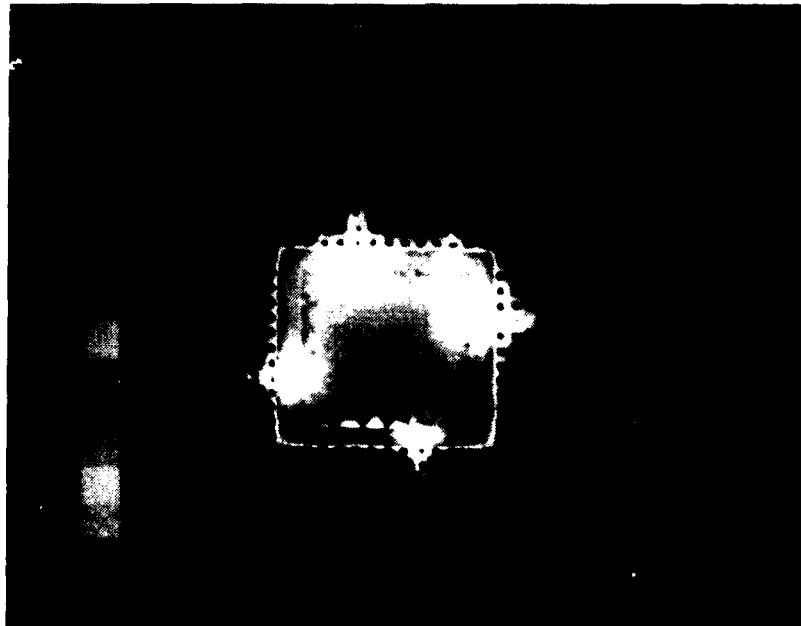


Figure 89. Pins 33, 82, 131 and 180 of F3, 5A total.

Table 13. Maximum Current of Power and Ground Leads.

<u>Lead No.</u>	<u>System</u>	<u>Max. Current (amps)</u>
9	GND	4.01
17	P2	4.23
25	P1	4.18
33	P3	4.14
41	GND	4.21
58	GND	4.52
66	P2	4.59
74	P1	5.08
82	P3	4.50
90	GND	5.15
107	GND	4.98
115	P2	4.21
123	P1	4.05
131	P3	4.17
139	GND	4.09
156	GND	4.10
164	P2	4.05
172	P1	3.98
180	P3	4.11
188	GND	3.96

#### 4.10 POWER AND GROUND NETWORK RESISTANCE MODEL

##### 4.10.1 Calculations of Structure Resistances

###### Package Leads

The resistances of a number of the leads of several packages were measured. This measurement was taken with a four-point probe from the tip of the lead to the braze pad of the package. From the data, the mean resistance of the leads was found to be 0.028 ohms.

###### Vias

The package vendor specified that the resistance of the vias is approximately 10 milliohms per layer. This specification is based on the via geometry and material. The vias are 8 mils in diameter and 8 mils deep per penetrated layer. The material of the vias is a tungsten thick film.

###### Power and Ground Plane Material

The power and ground planes are made of the same tungsten thick film material as the vias. The vendor specification calls for the planes to have a sheet resistance of 15 mohms per square. Using 10X artwork of the package, the number of squares between each node of the planes was found. The resistance between each node was calculated from the number of squares and the sheet resistance.

###### Seal Ring (Ground Network Only)

To find the resistance of the seal ring, the relation

$$R = \frac{pl}{A}$$

was used; where R = resistance in ohms, p = resistivity of Kovar in ohm-mils, l = length of resistor in mils, and A = cross sectional area of the seal ring in mils<sup>2</sup>. The resistivity of Kovar was found in the CRC Handbook of Chemistry and Physics to be 49 ohms-cm, which converts into 1.929E-02 ohm-mils. The cross-sectional area of the seal ring was found from the package drawings to be 1500 mils<sup>2</sup>, and the length of the seal ring between nodes was measured from the 10X artwork.

##### 4.10.2 Resistance Data

###### Labels

The resistors on the models are labeled as follows: RL\_\_ : Resistance of package leads; RV\_\_ : Resistance of vias; RP\_\_ : Resistance of plane material; RS\_\_ : Resistance of the seal ring (ground network only). The resistors are numbered sequentially, beginning with one (1), on each network.

Primary Power Plane - P1

<u>Resistor</u>	<u>Value (ohms)</u>	<u>Resistor</u>	<u>Value (ohms)</u>
RL1	0.028	RP16	0.029
RL2	0.028	RV17	0.010
RL3	0.028	RV18	0.010
RL4	0.028	RV19	0.010
RV5	0.020	RV20	0.010
RV6	0.020	RP21	0.1103
RV7	0.020	RP22	0.1103
RV8	0.020	RP23	0.1103
RV9	0.020	RP24	0.1103
RV10	0.020	RP25	0.1103
RV11	0.020	RP26	0.1103
RV12	0.020	RP27	0.1103
RP13	0.029	RP28	0.1103
RP14	0.029	RV29	0.005
RP15	0.029	RV30	0.005

Secondary Power Plane - P2

<u>Resistor</u>	<u>Value (ohms)</u>	<u>Resistor</u>	<u>Value (ohms)</u>
RL1	0.028	RP15	0.049
RL2	0.028	RP16	0.049
RL3	0.028	RV17	0.015
RL4	0.028	RV18	0.015
RV5	0.020	RV19	0.015
RV6	0.020	RV20	0.015
RV7	0.020	RP21	0.0745
RV8	0.020	RP22	0.1449
RV9	0.030	RP23	0.0745
RV10	0.030	RP24	0.1449
RV11	0.030	RP25	0.0745
RV12	0.030	RP26	0.1449
RP13	0.049	RP27	0.0745
RP14	0.049	RP28	0.1449



### Tertiary Power Plane - P3

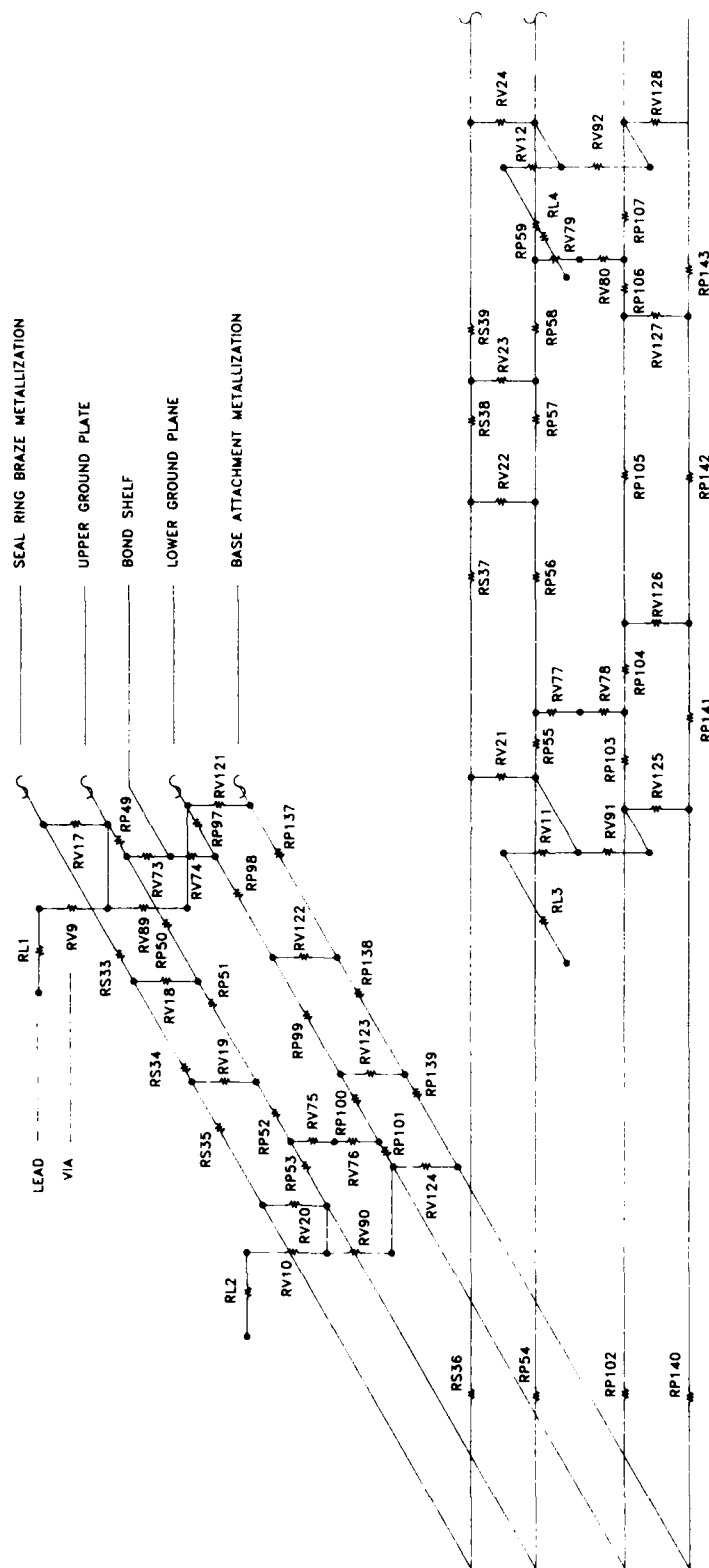
<u>Resistor</u>	<u>Value (ohms)</u>	<u>Resistor</u>	<u>Value (ohms)</u>
RL1	0.028	RP16	0.049
RL2	0.028	RV17	0.020
RL3	0.028	RV18	0.020
RL4	0.028	RV19	0.020
RV5	0.020	RV20	0.020
RV6	0.020	RP21	0.1103
RV7	0.020	RP22	0.0551
RV8	0.020	RP23	0.1103
RV9	0.040	RP24	0.0551
RV10	0.040	RP25	0.1103
RV11	0.040	RP26	0.0551
RV12	0.040	RP27	0.1103
RP13	0.049	RP28	0.0551
RP14	0.049	RV31	0.005
RP15	0.049		

### Ground Network

<u>Resistor</u>	<u>Value (ohms)</u>	<u>Resistor</u>	<u>Value (ohms)</u>
RL1	0.028	RV29	0.010
RL2	0.028	RV30	0.010
RL3	0.028	RV31	0.010
RL4	0.028	RV32	0.010
RL5	0.028	RS33	0.0018
RL6	0.028	RS34	0.0016
RL7	0.028	RS35	0.0018
RL8	0.028	RS36	0.0022
RV9	0.010	RS37	0.0018
RV10	0.010	RS38	0.0016
RV11	0.010	RS39	0.0018
RV12	0.010	RS40	0.0022
RP13	0.010	RS41	0.0018
RP14	0.010	RS42	0.0016
RP15	0.010	RS43	0.0018
RP16	0.010	RS44	0.0022
RV17	0.010	RS45	0.0018
RV18	0.010	RS46	0.0016
RV19	0.010	RS47	0.0018
RV20	0.010	RS48	0.0022
RV21	0.010	RP49	0.025
RV22	0.010	RP50	0.065
RV23	0.010	RP51	0.082
RV24	0.010	RP52	0.065
RV25	0.010	RP53	0.025
RV26	0.010	RP54	0.117
RV27	0.010	RP55	0.025
RV28	0.010	RP56	0.065

<u>Resistor</u>	<u>Value (ohms)</u>	<u>Resistor</u>	<u>Value (ohms)</u>
RP57	0.082	RP105	0.102
RP58	0.065	RP106	0.019
RP59	0.025	RP107	0.016
RP60	0.117	RP108	0.048
RP61	0.025	RP109	0.016
RP62	0.065	RP110	0.019
RP63	0.082	RP111	0.102
RP64	0.065	RP112	0.019
RP65	0.025	RP113	0.016
RP66	0.117	RP114	0.048
RP67	0.025	RP115	0.016
RP68	0.065	RP116	0.019
RP69	0.082	RP117	0.102
RP70	0.065	RP118	0.019
RP71	0.025	RP119	0.016
RP72	0.117	RP120	0.048
RV73	0.010	RV121	0.030
RV74	0.005	RV122	0.040
RV75	0.010	RV123	0.040
RV76	0.005	RV124	0.040
RV77	0.010	RV125	0.030
RV78	0.005	RV126	0.040
RV79	0.010	RV127	0.040
RV80	0.005	RV128	0.040
RV81	0.010	RV129	0.030
RV82	0.005	RV130	0.040
RV83	0.010	RV131	0.040
RV84	0.005	RV132	0.040
RV85	0.010	RV133	0.030
RV86	0.005	RV134	0.040
RV87	0.010	RV135	0.040
RV88	0.005	RV136	0.040
RV89	0.020	RP137	0.037
RV90	0.020	RP138	0.075
RV91	0.020	RP139	0.037
RV92	0.020	RP140	0.024
RV93	0.020	RP141	0.037
RV94	0.020	RP142	0.075
RV95	0.020	RP143	0.037
RV96	0.020	RP144	0.024
RP97	0.016	RP145	0.037
RP98	0.019	RP146	0.075
RP99	0.102	RP147	0.037
RP100	0.019	RP148	0.024
RP101	0.016	RP149	0.037
RP102	0.048	RP150	0.075
RP103	0.016	RP151	0.037
RP104	0.019	RP152	0.024

NOTE: SEE ATTACHED DATA SHEET FOR  
 RESISTOR VALUES  
 RL - PACKAGE LEAD RESISTANCE  
 RV - VIA RESISTANCE  
 RP - GROUND PLANE PLATING MATERIAL  
 RESISTANCE  
 RS - SEAL RING RESISTANCE



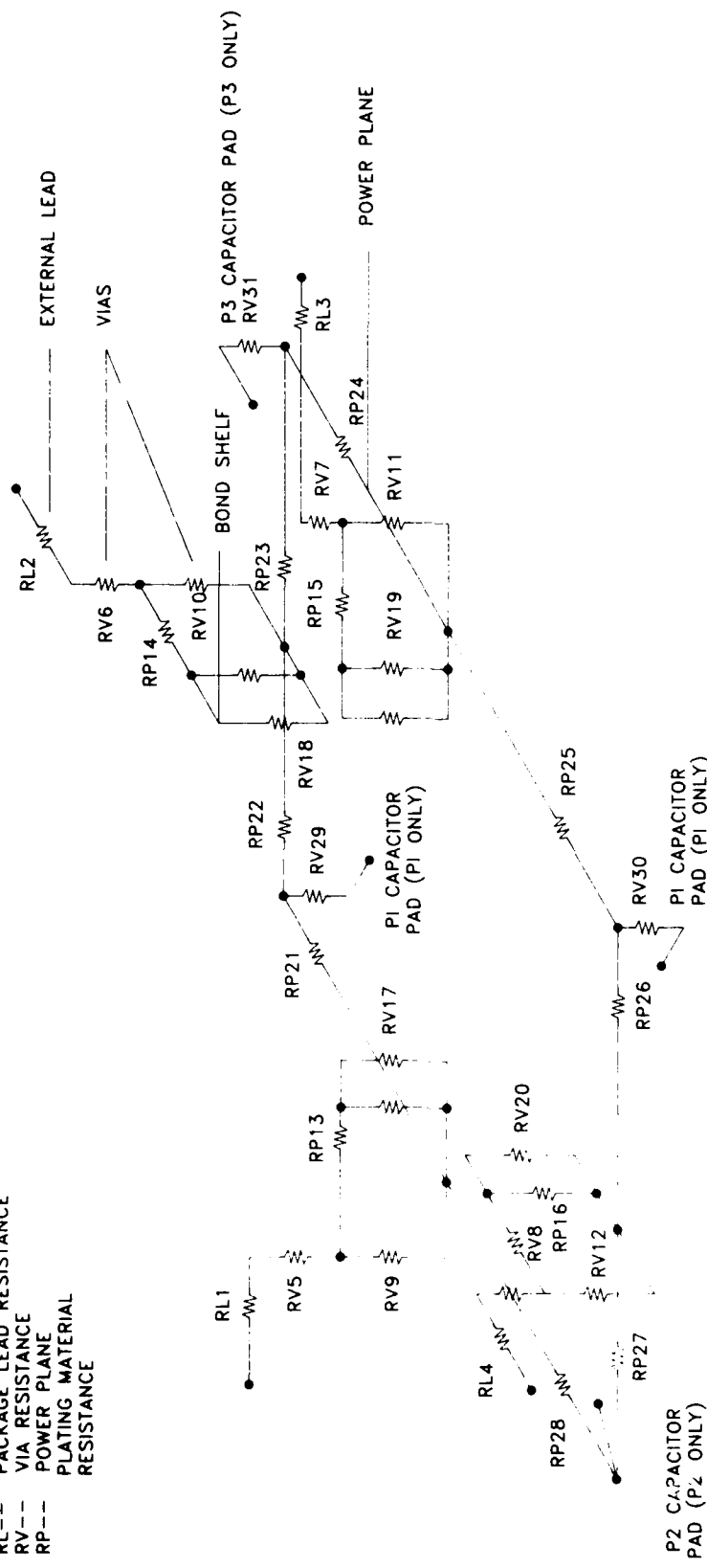
LABCOM - VMC  
 196 - PIN PACKAGE  
 1/2 RESISTANCE NETWORK MODEL FOR GROUND SYSTEM

A0176

Figure 90. Resistance network model for ground system.

NOTE: SEE ATTACHED DATA SHEET:

- RL-- FOR RESISTOR VALUES
- RV-- PACKAGE LEAD RESISTANCE
- RV-- VIA RESISTANCE
- RP-- POWER PLANE PLATING MATERIAL RESISTANCE



LABCOM - VMC  
196 - PIN PACKAGE  
RESISTANCE NETWORK FOR PRIMARY, SECONDARY, AND TERTIARY POWER PLANES

A0173

Figure 91. Resistance network model for primary, secondary and tertiary power planes.

## SECTION V

### 883 PACKAGE / LID EVALUATION

#### 5.0 INTRODUCTION

The objective of this effort was to determine the environmental integrity of both packages by testing for conformance to the package evaluation requirements as detailed in this section. The parts were tested to applicable MIL-STD-883 Methods in addition to being temperature cycled to evaluate any structural effects on the package itself. Additional temperature cycling and vibration testing were performed upon packages mounted to boards to test for adverse effects on the solder joints. The coefficient of thermal expansion of both packages and one lid size were characterized.

A test sequence was developed which would test both packages to the appropriate conditions of all applicable MIL-STD-883C methods. This included physical dimensions, solderability, thermal shock, stabilization bake, lead integrity, hermeticity, package isolation, moisture resistance and salt atmosphere. Physical dimensions were also taken for both lids.

#### 5.1 SUMMARY OF PACKAGE TEST SEQUENCE

Table 14 is a summary of the tests which were performed on the package, the method used and the number of samples tested. Physical dimensions of the lids were also taken per MIL-STD-883, method 2016.

Table 14. Package Test Sequence

Subgroup	Test	883 Method	Condition	Sample Size
1	Physical Dimensions	2016		15
2	Solderability	2003	SnPb at 245 +/- 5° C	3
3	Thermal Shock	1011	C	3
	Stabilization Bake	1008	24 hours at 150° C	3
	Lead Integrity	2004	B2, .229 +/- .014 kg, 3 cycles at 90°, 15 leads minimum	3
	Hermeticity	1014	A4	3
4	Package Isolation	1003	600 VDC, 100 nA minimum	3
5	Moisture Resistance	1004	10 cycles	5
6	Salt Atmosphere	1009	24 hours at 35° C	5
7	Plating Thickness	none	50 - 225 $\mu$ inches Au 50 - 350 $\mu$ inches Ni	100%
8	CTE Characterization	none	Cooling first, heating second	2
*	Random and Harmonic Vibration, packages assembled to board	none	One octave band, frequency centered around previously determined characteristic frequency, increase amplitude to failure	4
*	Temperature cycling, package assembled to board	none	-55 to 125° C to failure	4
*	Package hermeticity through temperature cycling	none	-55 to 125° C	6

## 5.2 PHYSICAL DIMENSIONS

### 5.2.1 Physical Dimensions - Packages

Twelve different dimensions were checked for a sample of fifteen pieces each of the two package sizes. A list describing these dimensions follows (see Figures 92 and 93 for pictorial representations of these dimensions for the 196 I/O and 308 I/O packages respectively):

- (A) Outside dimension of the seal ring
- (B) Width of the seal ring
- (C) Outside dimension of ceramic package body
- (D) Length of the top braze pad
- (E) Width of the top braze pad
- (F) Existence of index corner chamber (yes/no)
- (G) Inside dimension of lead frame tie bar
- (H) Dimension of first lead center line to last lead center line on a given side
- (I) Width of lead
- (J) Thickness of lead frame
- (K) Thickness of ceramic package body
- (L) Overall package thickness

A summary of the results of the package physical dimension verification is shown in Tables 15 and 16. Although fifteen pieces of each package type were examined, a greater number of measurements was taken depending upon the dimension being measured.

The number of measurements, mean value, standard deviation, and delta from the nominal value is shown in these tables with respect to the specified dimensions and allowable tolerance.

Method 2016 of MIL-STD-883C also calls for an external visual inspection. These results are noted in the following discussion.

One of the fifteen 196 I/O packages was classified as a failure due to contamination present within the package cavity. Ten of the fifteen packages were failed on dimension (G) which is the inside dimension of the lead frame tie bar. This was solely due to the fact that the lead frame was designed to a 1.950 nominal instead of a 1.950 minimum. At any rate, this did not result in any subsequent processing problem with the parts.

Two of the fifteen 308 I/O packages were classified as failures due to package cavity contamination. Also, as with the 196 lead package, thirteen of the fifteen packages tested failed on the inside dimension of the lead frame for the reason stated above. In addition, one out of fifteen failed on dimension (A) which is the outside dimension of the seal ring, four of fifteen failed on dimension (C) which is the outside dimension of the ceramic package body, and twelve of the fifteen failed on dimension (D) which is the length of the top braze pad. Dimensions (A) and (C) are somewhat critical and need to be worked with the package vendor but (D) is not critical and its tolerance can probably be loosened without any adverse effects.





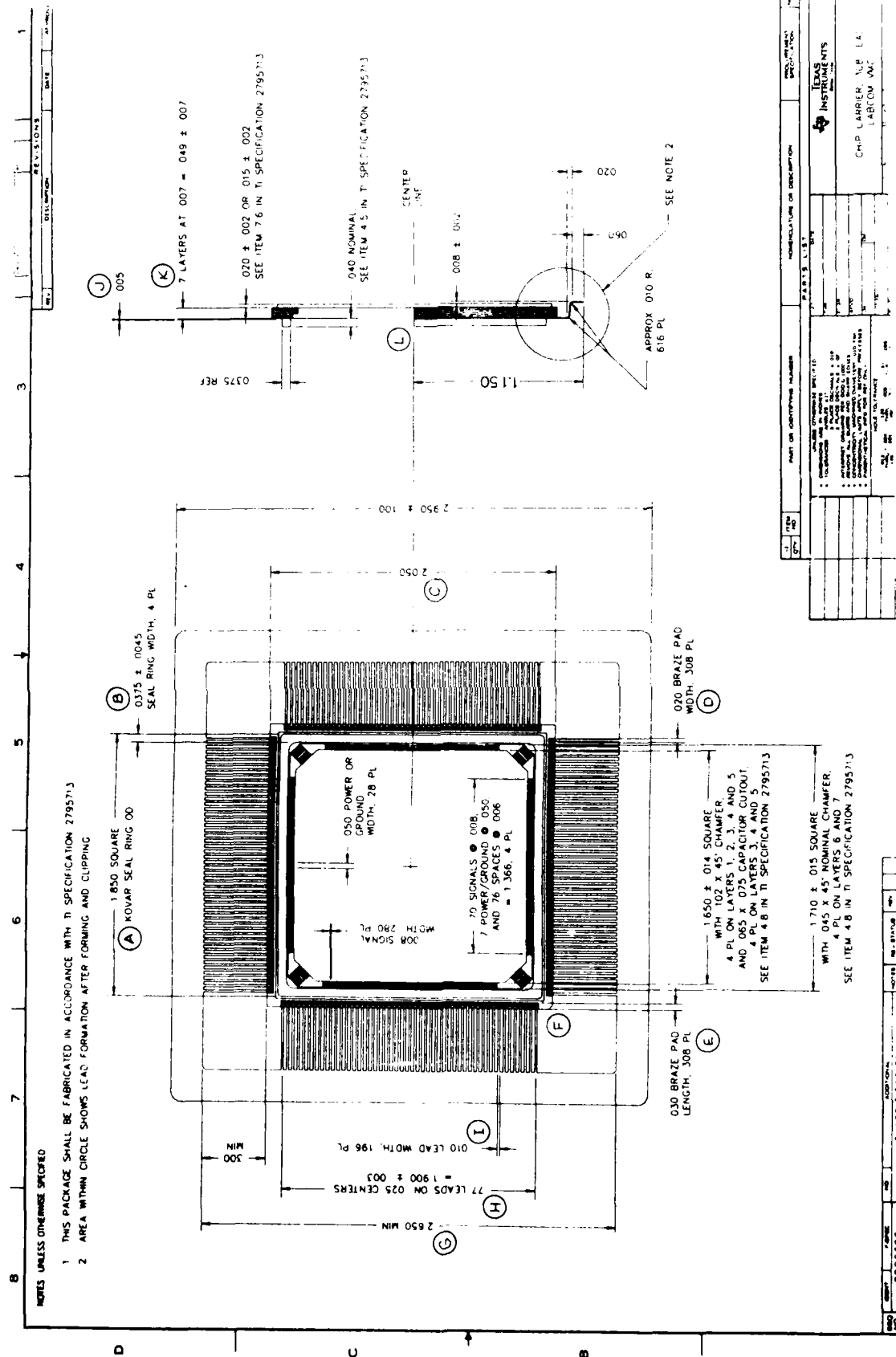


Figure 93. Package Dimensions of 308 I/O

Table 15. 196 Lead Package

DIMENSION	TOLERANCE	DELTA FROM NOMINAL	MEAN	STANDARD DEVIATION	NUMBER OF MEASURE- MENTS
(A) 1.250	+/- .010	+ .00126	1.25126	.00325	60
(B) .0375	+/- .0045	- .00177	.03573	.00171	60
(C) 1.350	+/- .011	+ .00099	1.35099	.00129	60
(D) 0.030	+/- .005	- .00232	.02768	.00381	28
(E) 0.020	+/- .005	+ .00057	.02057	.00042	28
(F) Yes					
*(G) 1.950	minimum	- .00071	1.94929	.00143	36
(H) 1.200	+/- .003	+ .00018	1.11018	.00275	60
(I) .010	+/- .005	- .00029	.00971	.00058	36
(J) .005	none	+ .00021	.00521	.00035	36
(K) .049	+/- .007	- .00037	.04863	.00016	60
(L) .115	maximum	- .00819	.10681	.00091	16

NOTE: \* indicates delta from nominal in excess of specified tolerance

Table 16. 308 Lead Package

DIMENSION	TOLERANCE	DELTA FROM NOMINAL	MEAN	STANDARD DEVIATION	NUMBER OF MEASURE- MENTS
(A) 1.850	+/- .015	+ .00607	1.85607	.00304	60
(B) .0375	+/- .0045	+ .00192	.03942	.00135	60
(C) 2.050	+/- .016	+ .00866	2.05866	.00334	60
*(D) 0.030	+/- .005	+ .00896	.03896	.00413	66
(E) 0.020	+/- .005	+ .00180	.02180	.00072	68
(F) Yes/No					
*(G) 2.650	minimum	- .00090	2.64910	.00163	30
(H) 1.900	+/- .003	- .00203	1.89797	.00234	58
(I) .010	+/- .005	- .00005	.00995	.00012	66
(J) .005	none	+ .00002	.00502	.00016	38
(K) .049	+/- .007	- .00198	.04702	.00083	60
(L) .115	maximum	- .00828	.10672	.00142	60

NOTE: \* indicates delta from nominal in excess of specified tolerance

### 5.2.2 Physical Dimension - Lids

Four different dimensions were checked for each of the two lids. A list describing these dimensions follows (see Figure 94 for a pictorial representation of these dimensions):

- (A) Lid length
- (B) Lid width
- (C) Lid overall thickness
- (D) Lid step thickness

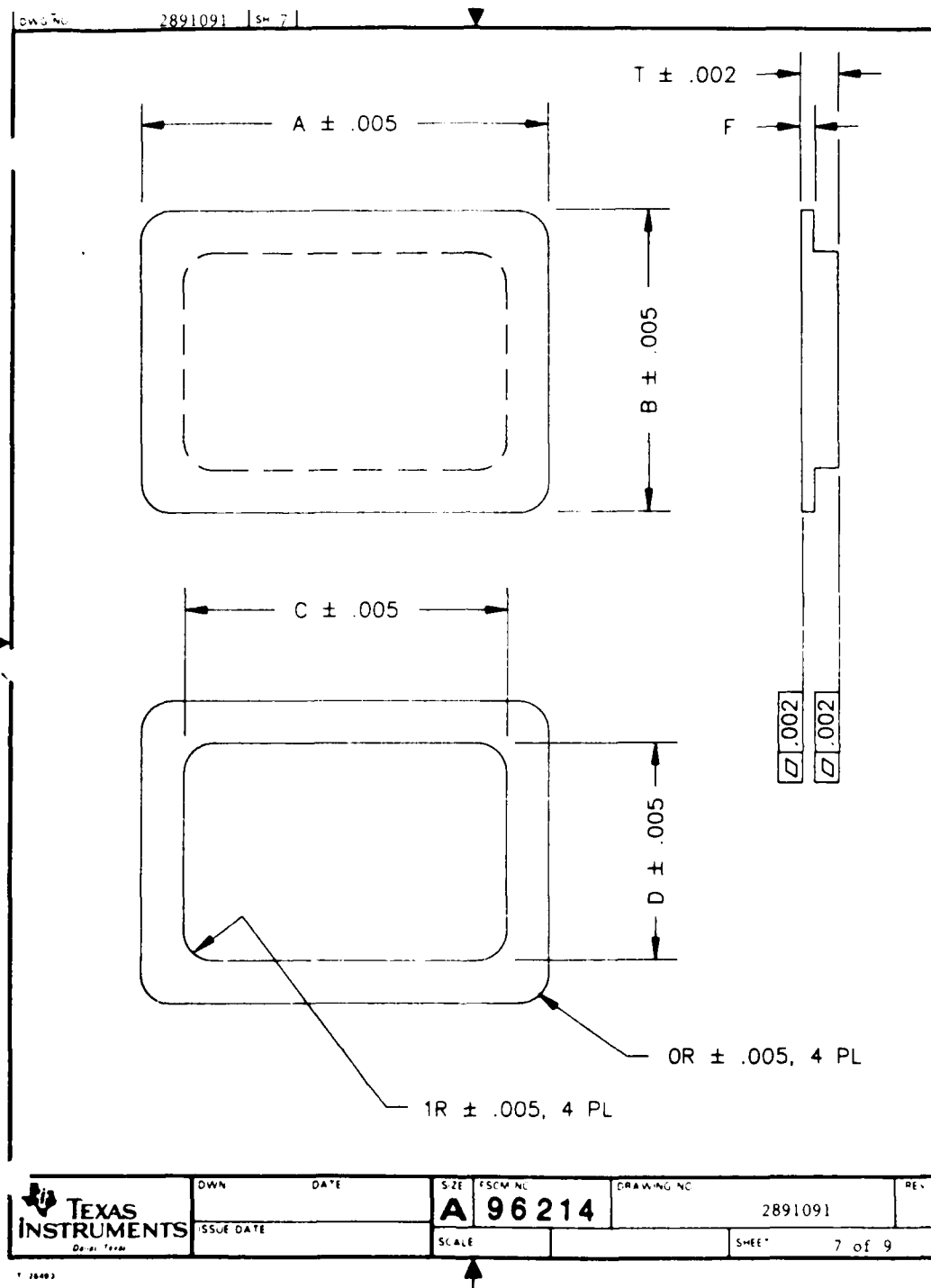


Figure 94. Lid Dimensions of 19C and 308 Lead Package

A summary of the results of the lid physical dimension verification is shown in Tables 17 and 18 for the 196 lead lid and 308 lead lid respectively. Fifteen pieces of each lid type were examined.

The number of measurements, mean value, standard deviation and delta from the nominal value is shown in these tables with respect to the specified dimension and allowable tolerance.

All lids tested were well within the specification.

Table 17. 196 Lead Package Lid

DIMENSION	TOLERANCE	DELTA FROM NOMINAL	MEAN	STANDARD DEVIATION	NUMBER OF MEASURE- MENTS
(A) 1.245	+/- .005	- .00047	1.24453	.00111	15
(B) 1.245	+/- .005	+ .00177	1.24677	.00112	15
(T) 0.015	+/- .002	- .00023	.01477	.00026	15
(F) 0.0045	+/- .001	+ .00050	.005	-0-	15

Table 18. 308 Lead Package Lid

DIMENSION	TOLERANCE	DELTA FROM NOMINAL	MEAN	STANDARD DEVIATION	NUMBER OF MEASURE- MENTS
(A) 1.845	+/- .005	- .00060	1.84440	.00188	15
(B) 1.845	+/- .005	- .00267	1.84233	.00129	15
(T) 0.015	+/- .002	- .00080	.01420	.00045	15
(F) 0.0045	+/- .001	+ .00037	.00487	.00037	15

### 5.3 SOLDERABILITY

#### 5.3.1 Introduction

The purpose of this test was to determine the solderability of the package leads. This determination is made on the basis of the ability of the leads to be wetted or coated by solder using a dip procedure. This testing verifies that the lead frames have been processed, i.e. plated, satisfactorily during fabrication to facilitate the formation of a solder connection. An accelerated aging test is included which simulates a minimum of six months natural aging under a combination of various storage conditions that have different deleterious effects. This is done through the use of an eight hour steam bath at 245° C. Failure criteria based on MIL-STD-883C, Method 2003.5 dictates that the total surface area of the dipped part of the termination is at least 95 percent covered by a continuous new solder coating and that pinholes, voids, porosity, nonwetting, or dewetting are not concentrated in one area and do not exceed 5 percent of the total area.

#### 5.3.2 Results

Three samples of each of the two package types were subjected to the solderability test and all passed. The lids were not subjected to solderability testing since they are not soldered onto the package assembly in its final form.

### 5.4 THERMAL SHOCK

#### 5.4.1 Introduction

The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature. These conditions may be encountered in equipment operated intermittently in low temperature areas. Permanent changes in operating characteristics and physical damage produced during temperature shock occur principally from stresses resulting from combinations of materials which have different coefficients of thermal expansions. Typical effects of thermal shock include cracking and delamination of substrates or wafers, opening of seals or seams, and changes in electrical characteristics due to moisture effects or to mechanical displacement of conductors or insulating materials. Failure criteria per MIL-STD-883C, Method 1011.7, Condition C consists of any evidence of defects or damage to the case, leads or seals after exposure to 15 cycles of -65° C to 150° C.

#### 5.4.2 Results

Three samples of each of the two package types were subjected to this thermal shock test and all passed.

## 5.5 STABILIZATION BAKE

### 5.5.1 Introduction

The purpose of this test is to determine the effect of storage at elevated temperatures without electrical stress applied. This method may also be used in a screening sequence or as a preconditioning treatment prior to the performance of other tests. The packages were stored per MIL-STD-883C, Method 1008.2 for 24 hours at 150° C.

### 5.5.2 Results

Three pieces of each of the two package types were subjected to the 24 hour stabilization bake and all passed.

## 5.6 LEAD INTEGRITY

### 5.6.1 Introduction

The purpose of this test is to determine the integrity of the package lead frames. MIL-STD-883C, Method 2004.5, Condition B2 employs multiple applications of bending stresses primarily to determine the resistance of the leads to metal fatigue under repeated bending. Condition B2 calls for the application of a 3 oz. force to each lead to be tested for three 90° arcs of the case.

### 5.6.2 Results

A minimum of fifteen leads were tested for each of three samples of the two package types. All leads passed this test.

## 5.7 HERMETICITY

### 5.7.1 Introduction

The purpose of this test is to determine the effectiveness of a device package seal. This test is performed per MIL-STD-883C, Method 1014.8, Condition A4, and is conducted on an unlidded package by placing the package, cavity down, over the evacuation port of a leak detector. A sound seal is created between the package and the leak detector through the use of a lubricated gasket. The external portion of the package is flooded with helium gas at a pressure of 30 psig and presence of helium is sensed inside the package by the leak detector. Failure occurs if the measured leak rate exceeds  $1 \times 10^{-8}$  atm cc/sec He.

### 5.7.2 Results

Three samples of each of the two package types were subjected to this hermeticity test and all passed.

## 5.8 PACKAGE ISOLATION

### 5.8.1 Introduction

This test is to measure the resistance offered by the insulating members of a component part to an impressed direct voltage tending to produce a leakage of current through or on the surface of these members. Insulation resistance measurements should not be considered the equivalent of dielectric withstanding voltage or electric breakdown tests. A clean, dry insulation may have a high insulation resistance, and yet possess a mechanical fault that would cause failure in the dielectric withstanding voltage test. Factors affecting insulation resistance measurements include temperature, humidity, residual charges, charging currents, etc. The specification for these packages is 100 nanoamps maximum at an applied voltage of 600 VDC.

### 5.8.2 Results

Due to the construction of the packages (i.e. plating tie bar shorting all electrical connections together), this test was not performed. It is anticipated that there will be no problem in meeting the specification based on readings from other fine pitch packages fabricated by the same package vendor.

## 5.9 MOISTURE RESISTANCE

### 5.9.1 Introduction

The moisture resistance test is performed for the purpose of evaluating, in an accelerated manner, the resistance of components to the deteriorative effects of the high-humidity and heat conditions typical of tropical environments. Most tropical degradation results directly or indirectly from absorption of moisture vapor and films by vulnerable insulating materials, and from surface wetting of metals and insulation. These phenomena produce many types of deterioration, including corrosion of metals and detrimental changes in electrical properties. This test, MIL-STD-883C, Method 1004.7, differs from the steady-state humidity test and derives added effectiveness in its employment of temperature cycling, which provides alternate periods of condensation and drying essential to the development of the corrosion processes. The test includes a low-temperature subcycle that acts as an accelerant to reveal otherwise indiscernible evidences of deterioration since stresses caused by freezing moisture tend to widen cracks and fissures. Results obtained with this test are reproducible and have been confirmed by investigations of field failures. Failure criteria per this MIL method classifies failures as the following:

- Missing, faded or otherwise illegible markings.
- Evidence of corrosion over more than 5 percent of the area of finished metal.
- Missing, broken or partially separated leads.
- Corrosion formations which bridge between leads or metal areas.
- Electrical end-point or insulation resistance test failures.

### 5.9.2 Results

Five samples of each of the two package types were subjected to ten cycles of the moisture resistance test and all passed.

## 5.10 SALT ATMOSPHERE

### 5.10.1 Introduction

This test is proposed as an accelerated laboratory corrosion test simulating the effects of seacoast atmosphere on devices and package elements. Per the appropriate conditions of MIL-STD-883C, Method 1009.6, the parts are subjected to a 35° C salt fog environment for 24 hours. Applicable failure criteria consists of the following:

- (a) Evidence of corrosion over more than five percent of the area of the finish or base metal of any package element or any corrosion that completely crosses the element
- (b) Leads that pass criteria cited in (a) but which exhibit electrochemical degradation (pinholes, pitting, blistering, flaking, etc.) shall be further tested as follows: bend the leads through 90 degrees at the point of degradation in such a manner that tensile stress is applied to the defect region - any lead which breaks or shows degradation of the base material that completely crosses the lead when viewed from directly above the defect shall be considered a reject
- (c) Leads missing, broken or partially separated

### 5.10.2 Results

Five packages were subjected to the salt atmosphere test as described above and three of the parts failed due to corrosion of metallized surfaces. This was expected to some degree due to the severity of the test and the stringency of the failure criteria. It was later determined that these sample parts did not contain a nickle flash and were not intended for salt atmosphere stressing.

## 5.11 PLATING THICKNESS

### 5.11.1 Introduction

Gold and nickel plating thicknesses were measured on a group of 27 packages in a combination of the two package types to verify conformance with the specified plating thicknesses. The specification on both package types was as follows:

Gold - 50  $\mu$ inches minimum, 225  $\mu$ inches maximum  
over Nickel - 50  $\mu$ inches minimum, 350  $\mu$ inches maximum

### 5.11.2 Results

Measurement readings were taken at four points on each part and averaged. The results of the test are as shown in Table 19.



Table 19. Plating Thickness

	GOLD THICKNESS $\mu$ IN	NICKEL THICKNESS $\mu$ IN
SAMPLE 1	169	117
SAMPLE 2	126	109
SAMPLE 3	187	56
SAMPLE 4	114	163
SAMPLE 5	107	94
SAMPLE 6	190	49 *
SAMPLE 7	40 *	47 *
SAMPLE 8	122	134
SAMPLE 9	224	37 *
SAMPLE 10	100	37 *
SAMPLE 11	198	42 *
SAMPLE 12	72	46 *
SAMPLE 13	196	71
SAMPLE 14	105	68
SAMPLE 15	136	125
SAMPLE 16	125	107
SAMPLE 17	97	55
SAMPLE 18	146	102
SAMPLE 19	159	145
SAMPLE 20	109	54
SAMPLE 21	127	130
SAMPLE 22	69	81
SAMPLE 23	100	46
SAMPLE 24	191	51
SAMPLE 25	135	97
SAMPLE 26	121	157
SAMPLE 27	76	30 *
MEAN	131.15	83.33
STANDARD DEVIATION	45.60	40.68
FAILURES (%)	1	6

NOTE: Failures are denoted by asterisk (\*) in data listing, all failures were due to underplating.

## 5.12 CTE CHARACTERIZATION

### 5.12.1 Introduction

Testing was performed in the Mechanical Engineering Lab at Texas Instruments to determine the coefficient of thermal expansion (CTE) of the 196 I/O package and the 308 I/O package as well as a 308 I/O package lid. The purpose of the test was to establish a database for CTE on VHSIC chip carriers.

### 5.12.2 Test Procedure

The procedure listed below was used to measure the CTE on all three parts mentioned above.

1. One 308 I/O chip carrier, one 196 I/O chip carrier and a 308 I/O chip carrier lid were the test samples used in this characterization.
2. Micro-Measurements WK-00-125MG-350 strain gauges were used for this test. The WK series gauge was selected for its wide temperature range and environmental resistance capabilities. This strain gauge also features a dual-grid resistance pattern which ensures that, when separated, each gauge will be matched in apparent strain characteristics, as in all other properties.
3. The matching gauge patterns were separated into two separate. One served as the active gauge on the test sample and the other was mounted on titanium silicate to be used as a temperature compensation gauge.
4. Ten locations were selected to mount the active legs (See Figures 95 and 96). Two were placed at a right angle to one another inside each package (where a chip would normally be mounted). Two more were mounted on the outside of each package, back-to-back of the mounted gauge on the inside. In addition, two were placed back-to-back on a 308 I/O lid.
5. The gauge locations were degreased, lightly sanded and chemically cleaned to prepare the surfaces for bonding.
6. A heat-curing epoxy was used to adhere them to the test samples. Micro-Measurements M-Bond 600 was selected for its wide temperature range. They were bonded in place according to the standard procedure called out in Micro-Measurements Instruction Bulletin B-130-10. The epoxy was cured for two hours at 325° F and post-cured at 400° F for two more hours.
7. In a similar manner, the matching or compensation components were bonded to a titanium silicate with the M-Bond 600 epoxy.
8. The gauges were configured in a Wheatstone bridge circuit (half-bridge configuration), with each active gauge wired in the tension leg and each compensation gauge wired in the compression leg. This is done to compensate for the error due to the apparent strain. The active or positive leg of the bridge produces a strain reading due to thermal loading combined with apparent strain and the compression or negative leg produces a reading due to the apparent strain of the matching gauge only, since the CTE of titanium silicate is negligible. The output due to the apparent strain in the two cancels electrically and only the strain due to the thermal expansion of the test part is measured.

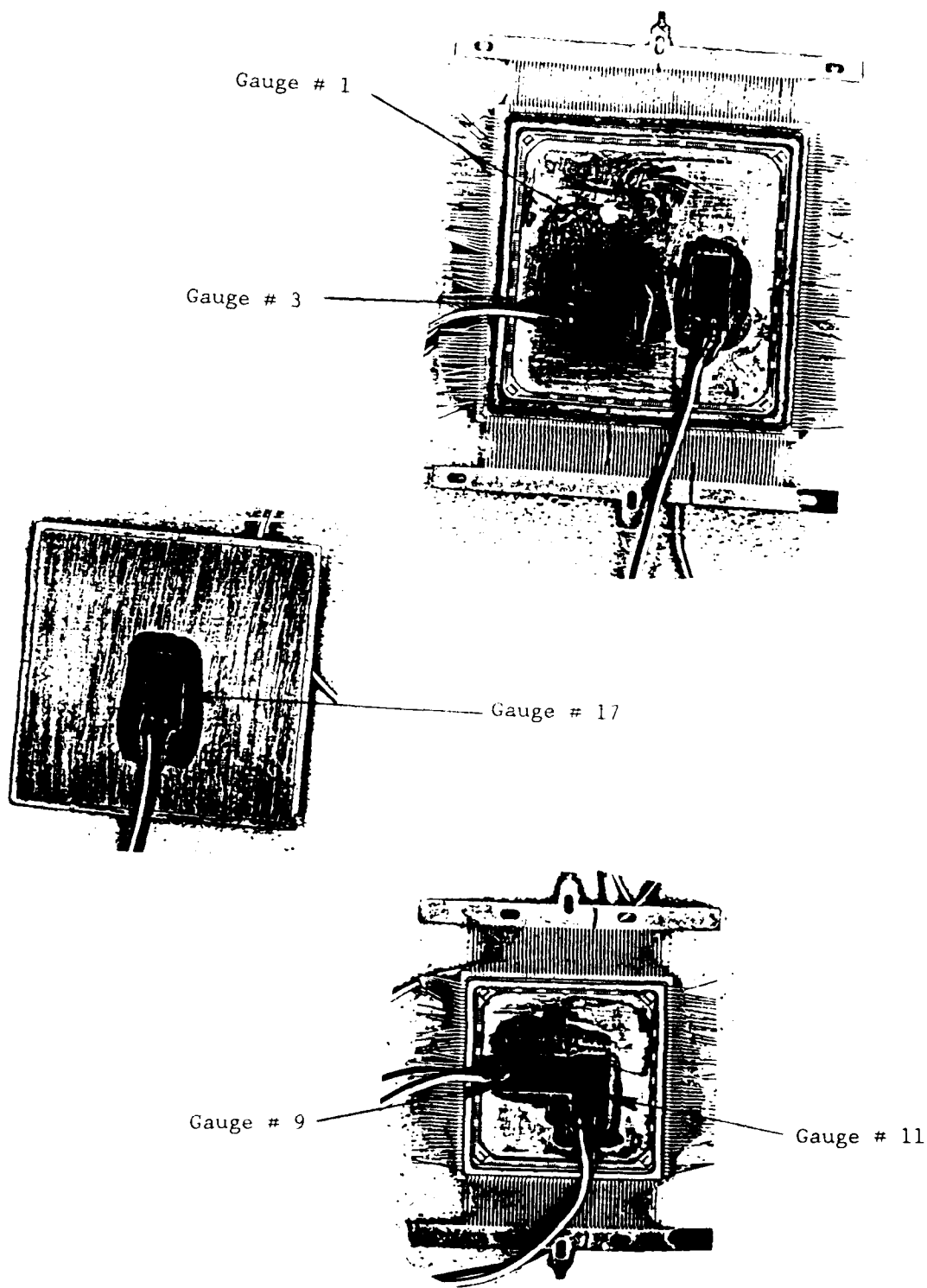


Figure 95. Strain Gauge Locations

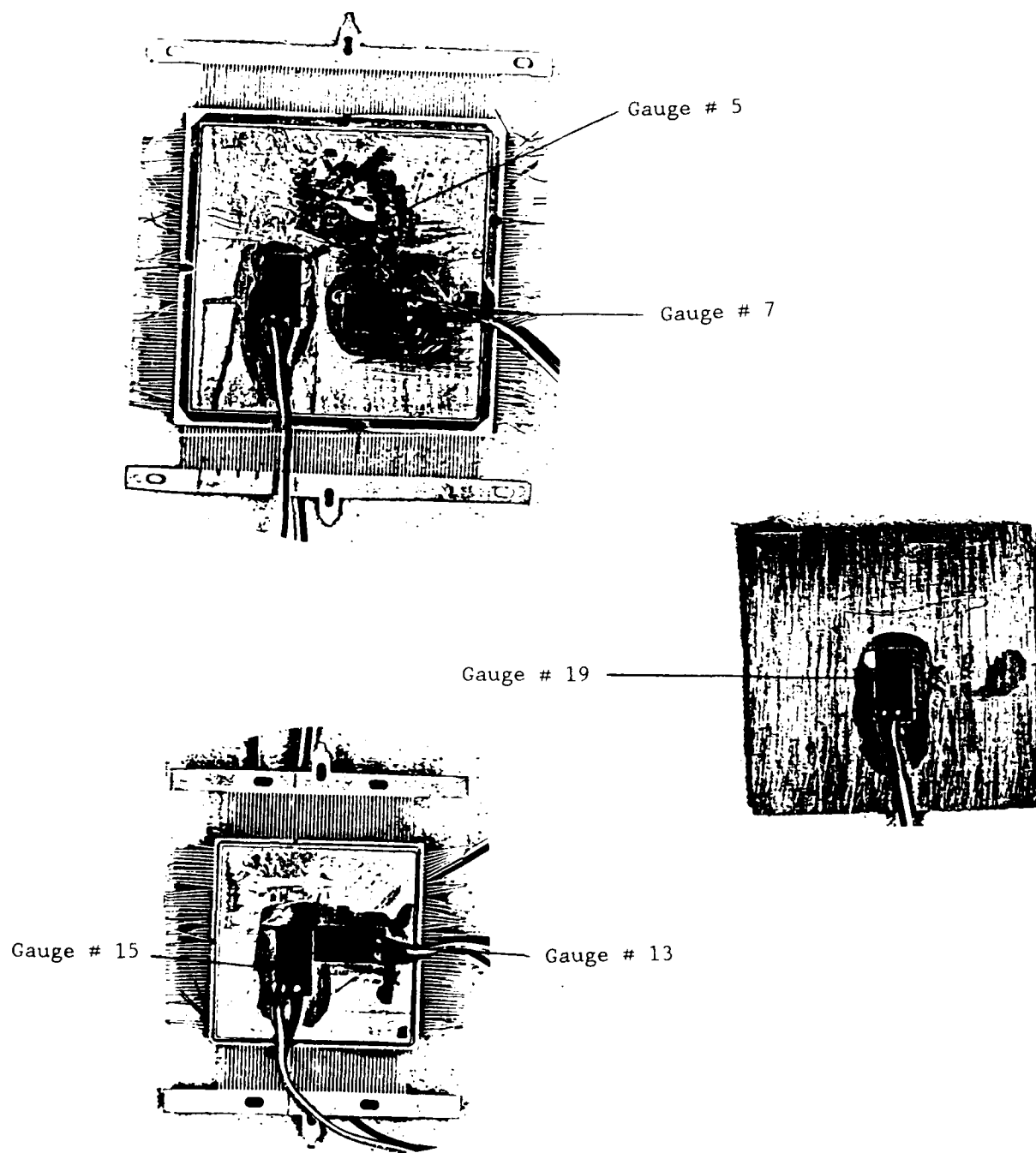


Figure 96. Strain Gauge Locations

9. Thermocouples were attached with thermal RTV and copper tape on the two packages, the lid and the titanium silicate to monitor the sample temperatures during the test.
10. The bridge circuits were wired into input connectors which were installed in the Solartron datalogger. The test samples were then placed in an environmental chamber. The datalogger was turned on and, after an initial warm-up period, all were balanced (zero strain) at room temperature (23° C).
11. The samples were allowed to thermal stabilize at selected temperatures. The Solartron Datalogger recorded all strain values and part temperatures at each stabilized point. The order and values of the temperatures selected for this test were: 23, -60, -50, -20, 0, 20, 40, 60, 80, 100, 120 and 23° C.
12. The test samples were cycled through all stabilized points three times to stabilize any hysteresis present in the gauge installation. All strain and temperature values were recorded for each stabilized point.
13. After being satisfied that the data was repeatable, the test samples were again cycled three times through all the stabilized points and data recorded for each temperature.
14. The strain and thermocouple measurements from the last three cycles were loaded into a LOTUS spreadsheet. The strain values from back-to-back were averaged to minimize errors due to test sample warpage during temperature cycling. CTEs were calculated based on the following formula.

$$\text{CTE} = \frac{\text{Difference in strain between stabilized readings}}{\text{Difference in temperature between stabilized readings}}$$

#### 5.12.3 Equipment

A list of the equipment used in this testing follows:

Solartron 3530E Datalogger  
 Texas Instruments Professional Computer  
 LOTUS 1-2-3 Software  
 Associated Oven  
 Micro-Measurements WK-00-125MG-350 Strain Gauges, Lot # DU-K06FA12

#### 5.12.4 Results

Three runs over the full temperature range were performed on each of the two package types. Table 20 shows the individual and averaged strain gauge values, individual and averaged thermocouple values, and average CTEs for a single test run on the 196 lead package. Table 21 shows the same information for a similar run on the 308 lead package and Table 22 shows information for a run on the 308 lead package lid.

Table 20. 196 Lead Package CTE Data

STRAIN GAUGE #1 $\mu\text{E}$	STRAIN GAUGE #2 $\mu\text{E}$	STRAIN GAUGE #3 $\mu\text{E}$	STRAIN GAUGE #4 $\mu\text{E}$	AVERAGE STRAIN $\mu\text{E}$	TC TEMP #1 $^{\circ}\text{C}$	TC TEMP #2 $^{\circ}\text{C}$	AVERAGE TEMP $^{\circ}\text{C}$	AVERAGE CTE in/in $^{\circ}\text{C}$
-0.9	-0.6	-0.2	-0.5	-0.55	22.6	22.7	22.65	
-495.3	-470.3	-513.0	-479.5	-489.68	-60.2	-60.0	-60.10	5.91
-437.1	-416.4	-454.6	-427.0	-433.78	-50.6	-50.5	-50.55	5.85
-376.9	-360.4	-393.3	-371.6	-375.55	-40.7	-40.5	-40.60	5.85
-256.8	-246.1	-268.4	-258.0	-257.33	-20.6	-20.5	-20.55	5.89
-138.9	-133.5	-146.5	-143.6	-140.63	-0.7	-0.6	-0.65	5.86
-23.1	-22.0	-25.2	-25.3	-23.90	19.1	19.2	19.15	6.30
91.4	91.3	95.3	96.9	93.73	38.9	39.1	39.00	5.92
208.8	210.0	219.7	222.6	215.28	59.1	59.2	59.15	6.03
328.5	330.0	340.1	345.2	335.95	78.7	78.9	78.80	6.14
444.6	446.7	459.2	466.9	454.35	97.9	98.1	98.00	6.16
563.9	567.4	582.4	592.2	576.48	117.6	117.7	117.65	6.21
623.1	626.8	642.6	654.7	636.80	127.4	127.5	127.45	6.15
683.6	686.1	702.0	717.0	697.18	137.0	137.1	137.05	6.29
2.9	2.2	0.9	2.8	2.20	22.9	23.1	23.00	6.09

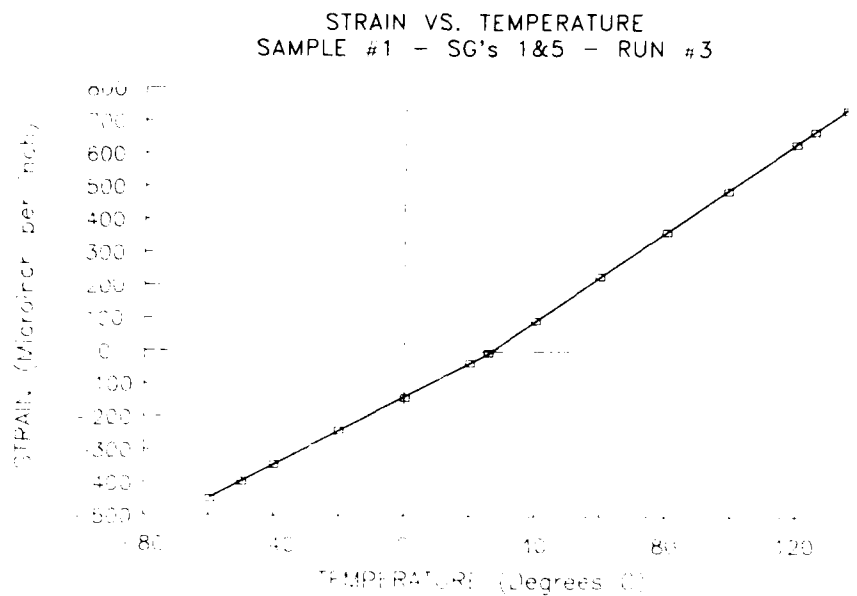
Table 21. 308 Lead Package CTE Data

STRAIN GAUGE #1 $\mu\text{E}$	STRAIN GAUGE #2 $\mu\text{E}$	STRAIN GAUGE #3 $\mu\text{E}$	STRAIN GAUGE #4 $\mu\text{E}$	AVERAGE STRAIN $\mu\text{E}$	TC TEMP #1 $^{\circ}\text{C}$	TC TEMP #2 $^{\circ}\text{C}$	AVERAGE TEMP $^{\circ}\text{C}$	AVERAGE CTE in/in $^{\circ}\text{C}$
-0.4	-0.1	-0.4	-0.1	-0.25	22.5	22.6	22.55	
-437.5	-547.6	-485.0	-435.0	-476.27	-60.3	-60.2	-60.25	5.75
-390.6	-485.7	-430.9	-381.4	-422.15	-50.7	-50.6	-50.65	5.64
-341.6	-420.6	-372.1	-327.7	-365.50	-40.8	-40.7	-40.75	5.72
-237.0	-286.1	-254.7	-223.6	-250.35	-20.7	-20.6	-20.65	5.73
-130.7	-155.1	-139.1	-121.3	-136.55	-0.8	-0.7	-0.75	5.72
-23.7	-28.5	-20.1	-17.0	-22.32	19.1	19.1	19.10	5.75
90.9	89.9	97.1	94.6	93.12	38.9	39.0	38.95	5.82
207.9	209.3	222.1	211.9	212.80	59.2	59.2	59.20	5.91
319.4	332.3	355.6	330.9	343.55	78.9	78.9	78.90	6.18
432.2	452.7	484.6	447.3	454.20	98.2	98.3	98.25	6.18
550.6	575.4	613.7	568.3	577.00	118.0	118.0	118.00	6.22
609.5	636.1	677.3	627.8	637.67	127.8	127.9	127.85	6.16
669.0	698.2	742.1	686.9	699.05	137.5	137.6	137.55	6.33
2.3	2.2	0.4	4.3	2.30	22.8	22.9	22.85	6.07

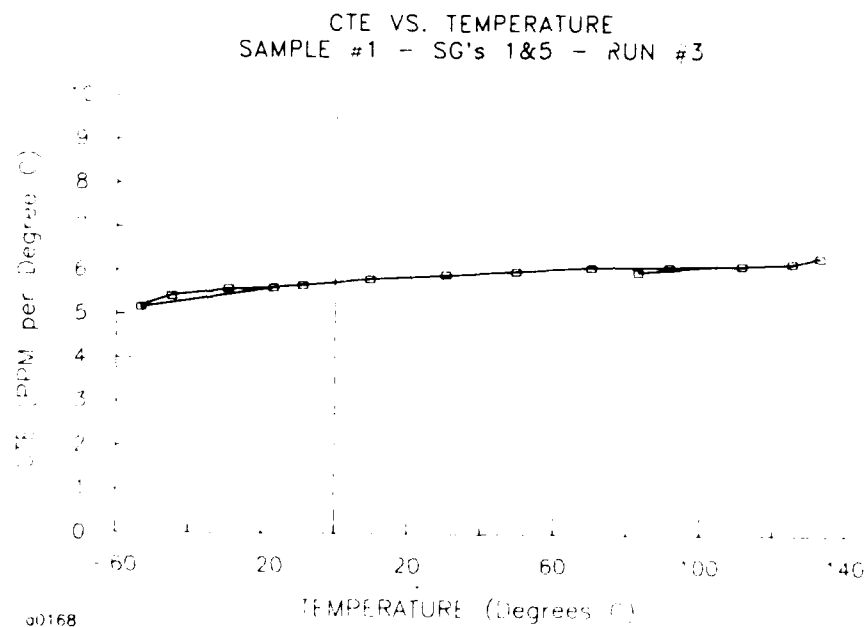
Table 22. 308 Lead Package Lid CTE Data

STRAIN GAUGE #1 $\mu\text{E}$	STRAIN GAUGE #2 $\mu\text{E}$	AVERAGE STRAIN $\mu\text{E}$	AVERAGE TEMP $^{\circ}\text{C}$	AVERAGE CTE in/in $^{\circ}\text{C}$
-0.7	-0.2	-0.5	22.5	
-785.6	-508.8	-647.2	-60.3	7.8
-696.9	-440.4	-568.7	-50.7	8.2
-600.1	-371.9	-486.0	-40.8	8.3
-399.9	-248.5	-324.2	-20.7	8.1
-207.1	-134.7	-170.9	-0.8	7.7
-34.1	-24.2	-29.2	19.1	7.2
112.0	65.9	89.0	38.9	5.9
247.0	128.2	187.6	59.2	4.9
374.9	187.0	281.0	78.9	4.8
492.2	249.1	370.7	98.2	4.7
608.1	312.8	460.5	118.0	4.5
663.7	338.7	501.2	127.8	4.2
717.4	358.2	537.8	137.5	3.8
1.2	-1.5	-0.2	22.8	4.7

The CTE was also plotted against the average temperature over which the measurements were taken. In addition, the recorded strain values were plotted versus the temperature at which they were measured. A representative plot of this information is shown as Figure 97 for the 196 lead package, as Figure 98 for the 308 lead package and as Figure 99 for the 308 lead package lid.



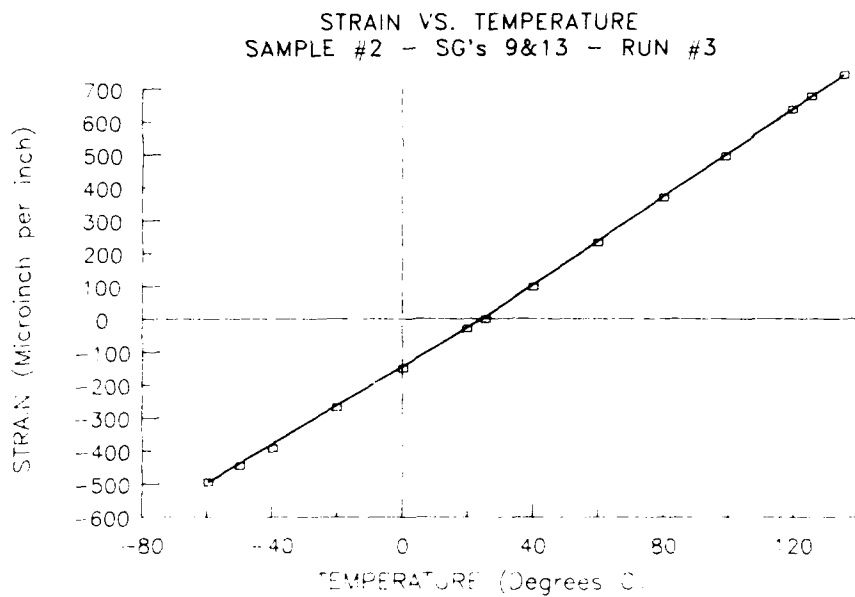
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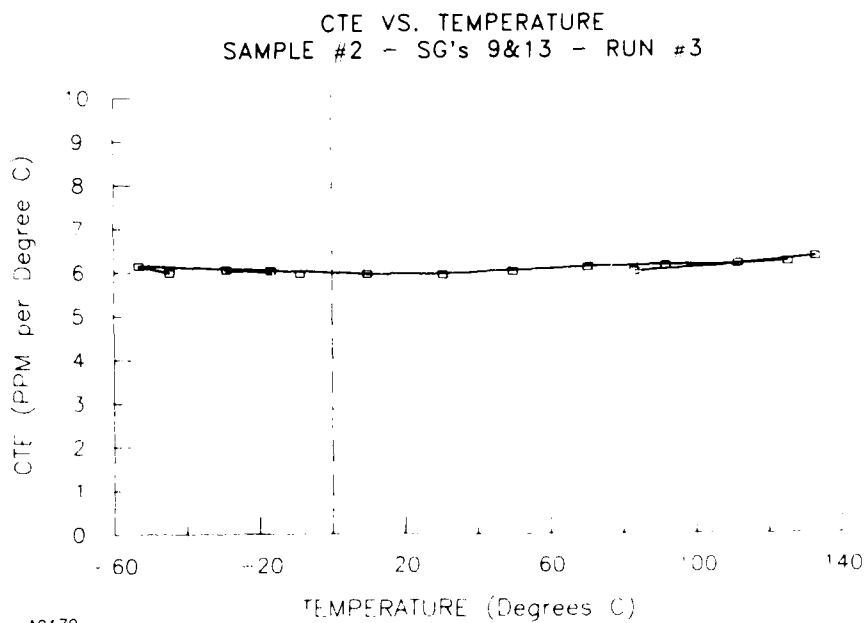
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Figure 97. 196 I/O Package Plot.



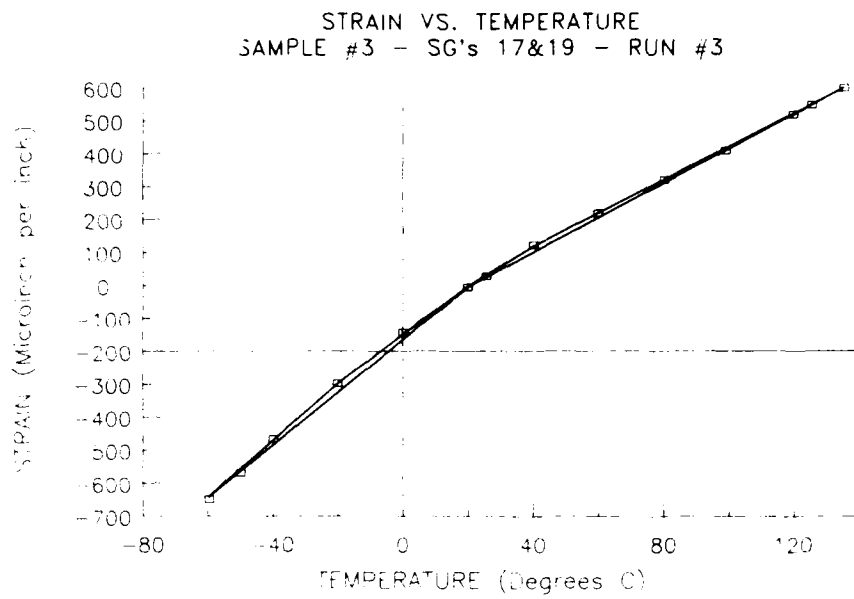


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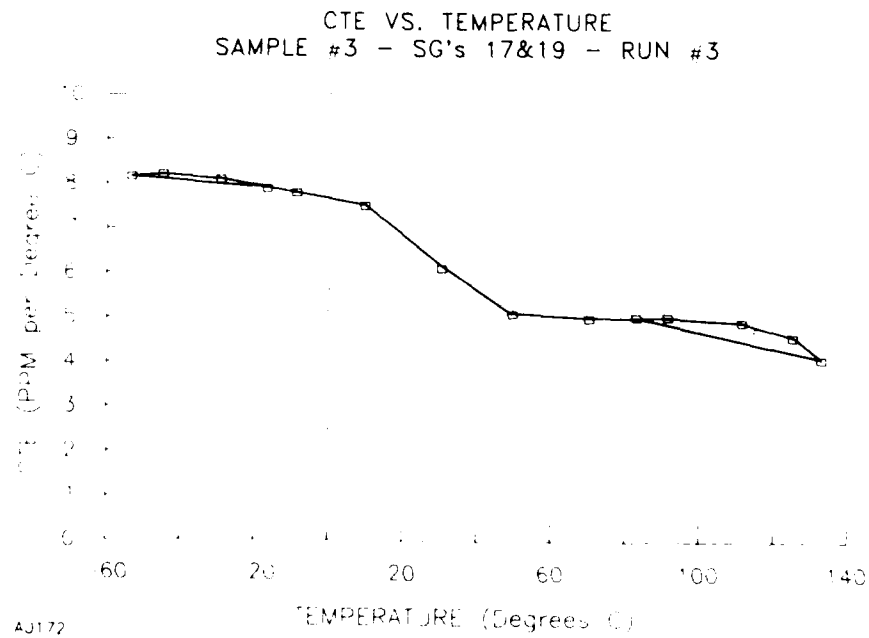


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Figure 98. 308 I/O Package Plot.



A0171



AJ172

Figure 99. 308 I/O Package Lid Plot.

## 5.13 RANDOM AND HARMONIC VIBRATION OF PACKAGE ASSEMBLED TO BOARD

### 5.13.1 Introduction

The purpose of this testing was to determine the resistance to vibration induced stresses of a package mounted on a board. Three packages of each of the two types were mounted to standard PWBS and tested under random and harmonic vibration to failure.

### 5.13.2 Test Sequence and Results

In order to perform this test, a baseline PWB was fabricated from G-10 with a top metallization pattern which would serve as a package mounting pad pattern and a daisy chain resistance circuit to monitor solder joint integrity during testing. The organic board was then laminated to a constraining metal plane which is representative of the type of board the package would actually be mounted on in a working system. In its unpopulated state, this board was randomly and harmonically vibrated to determine its characteristic vibration frequency. The natural frequency of the board was found to be 344 Hz and the transmissibility was 26.53.

Based on the information found in testing of the unpopulated board, the vibration test was designed to be within the range of expected failure. All testing was done in the z-axis only. Test results are given in Table 23.

TABLE 23. VIBRATION TEST PLAN

	PSD	TIME
Test #1	.01 G <sup>2</sup> /Hz	10 hours
Test #2	.04 G <sup>2</sup> /Hz	5 hours
Test #3	.20 G <sup>2</sup> /Hz	1 hour
Test #4	.40 G <sup>2</sup> /Hz	until failure

All boards were assembled using Raychem's Solder Quik as a means of attaching the package to the board. For boards #1 and #2 of each package type, packages were assembled to the board using a vapor phase reflow method such that the backsides of the packages were soldered down as a thermal joint. For Board #3 of each package type, the package was assembled to the board using hot bar reflow such that the backside of the body of the package was not mechanically attached to the board. After package mounting, the assemblies were conformably coated using Dow Corning DC 1-2577 silicone coating (a photograph of a 308 lead package board is shown as Figure 100). The six boards were then tested as detailed above with results as shown in Table 24.

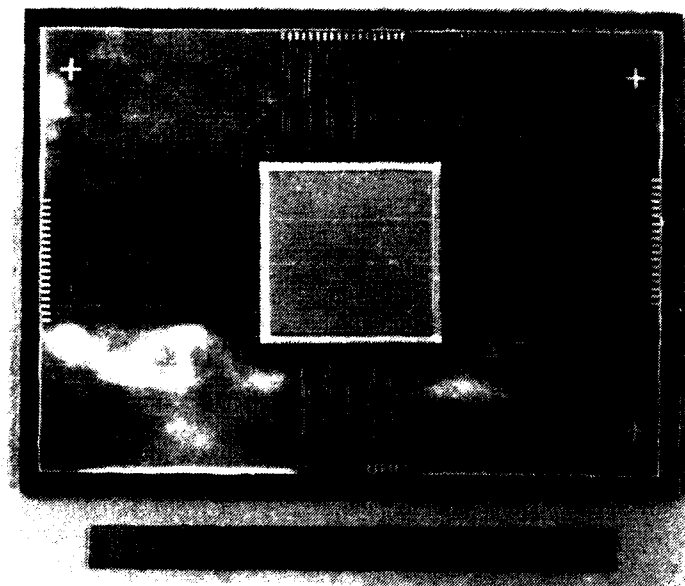


Figure 100. Random Vibration.

Table 24. Vibration Results

PACKAGE/ BOARD #	.01 G2/Hz (10 hours)	.04 G2/Hz (5 hours)	.20 G2/Hz (1 hour)
196 / #1	Passed	Passed	Joints failed, Package did not come off
196 / #2	Passed	Passed	Joints failed, Package did not come off
196 / #3	Passed	One joint failed, others OK	Package came off in 30 minutes
308 / #1	Passed	Joints failed	Package came off in 15 minutes
308 / #2	Passed	Package came off in 4 hours	
308 / #3	Passed	Package came off in 4 hours	

In the case of the 196 lead package, all boards passed Test #1 without any significant increase in resistance. Test #2 was also survived by all boards with the exception of one solder joint on Board #3. During Test #3, the package on Board #3 came off the board. This is the package which had been mechanically attached only at the lead frame, i.e. the package backside had not been soldered to the board. In this case the failure was due not to the solder joints but to the breakage of leads at the lead/package interface. Packages on the other two test boards remained in place, however there were many open joints and testing was terminated.

Results were similar for the 308 lead package assemblies, but somewhat accelerated due to the larger package size. All boards passed Test #1 but both Boards #2 and #3 lost their packages four hours into Test #2. Board #3 was the one which was assembled without the backside of the package being soldered to the board. Some joints failed on Board #1 during Test #2 but the package did not delaminate from the board until fifteen minutes into Test #3. As with the 196 lead package boards, failures occurred only due to breakage of leads, not to failure of solder joints.

#### 5.14 TEMPERATURE CYCLING OF PACKAGE ASSEMBLED TO BOARD

##### 5.14.1 Introduction

The purpose of this effort was to determine the long term reliability of the package/board mount while subjected to temperature and CTE mismatch induced stresses over the MIL temperature range, i.e. -55° C to 125° C.

##### 5.14.2 Test Sequence and Results

This testing was performed on boards of the type used in the vibration testing described in Section 5.13. Two packages of each type were tested - one which was mounted using a vapor phase reflow such that the package backside was attached to the board, the other using a hot bar reflow in which the backside of the package was not soldered to the board. The package/board assemblies were cycled from -55 to 125° C for 1000 cycles.

Although the hot bar reflowed package assembly still tested "good" at the low temperature after 1000 cycles, both of the 308 lead package assemblies failed earlier at ambient and hot conditions at 750 cycles. The vapor phase reflowed assembly failed at the low temperature at 900 cycles. There were no failures experienced on the two 196 lead package assemblies.

#### 5.15 PACKAGE HERMETICITY THROUGH TEMPERATURE CYCLING

##### 5.15.1 Introduction

The purpose of this test is to determine the effectiveness of the seal of a device package throughout exposure to the MIL temperature range. Like the testing detailed in Section 5.7 of this report, this test is conducted on an unlidded package by placing the package, cavity down, over the evacuation port of a leak detector. A sound seal is created between the package and the leak

detector through the use of a lubricated gasket. The external portion of the package is flooded with Helium gas at a pressure of 30 psig and presence of Helium is sensed inside the package by the leak detector. In this case, the failure criteria was a measured leak rate in excess of  $5 \times 10^{-8}$  atm cc/sec He.

#### 5.15.2 Results

Five sample 196 lead packages and eight sample 308 lead packages were tested for hermeticity after exposure to temperature cycling from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Results of this testing are shown in Table 25.

Table 25. Hermeticity After Temperature Cycling

NUMBER OF CYCLES	196 LEAD PACKAGE	308 LEAD PACKAGE
	# FAILURES / # SAMPLES	# FAILURES / # SAMPLES
0	5	8
10	1 / 6	2 / 8
50	1 / 5	1 / 6
100	0 / 4	1 / 5
TOTAL	2 / 6	4 / 8

## SECTION VI

### INTERAMICS PACKAGE FABRICATION YIELD ENHANCEMENT

#### 6.0 INTRODUCTION

The purpose of this segment of the program was to address some of the problems encountered by Interamics during the fabrication of the packages for Phase I of the VHSIC Multichip Packaging program. Six major areas of concern were identified as significant contributors to yield losses and quality problems. These were (a) foreign particles on wirebond pads, (b) lamination techniques and tools, (c) optimization of firing rate, (d) seal ring tooling, (e) shrinkage control and (f) conversion to production tooling. A discussion of these six tasks follows as subsections 6.1 through 6.6 and includes a detailed statement of each problem, actions taken, results and conclusions.

#### 6.1 FOREIGN PARTICLES (CERAMIC) ON WIREBOND PADS

##### 6.1.1 Statement of Problem

Foreign particles can damage the product through two different mechanisms. Those particles which are present during lamination become embedded into whatever surface upon which they are resting. This is not usually noticeable on the ceramic surfaces, but it is evident on metallized surfaces and can irreparably damage the metallization, particularly on wire bond fingers. If the particle "burns out" during firing (i.e. it is not a ceramic particle), then a dent or hole is left behind. If the particle is composed of ceramic and therefore will not burn out, the firing will bond the ceramic to the metallization. Since ceramic is nonconductive, subsequent plating operations will not cover the particle. The result is a plating void.

Particles which fall onto metallized surfaces after lamination, but before firing, will damage the product only if a nonconductive residue remains after firing. Generally, the particle is composed of ceramic and also will leave plating voids.

##### 6.1.2 Background

During Phase I, approximately 20 percent of the product was rejected for problems which were directly attributable to surface contamination by ceramic particles (alumina) in critical areas of the package. Particles such as this can cause voids in the final gold plating as well as raised bumps on metallized surfaces which interfere with the wire bonding process. In order to increase yields, it is necessary to isolate the source of these ceramic particles and to take corrective measures to reduce the number of reject parts. Current co-fire technology processes are highly susceptible to the generation of debris, most notably during the card cutting (blanking), via punching, cavity punching and lamination operations. While it is improbable that this problem can be completely eliminated, significant improvement in yields should be possible by making modifications to the processes involved. Interamics proposed to make two assembly starts of fifty dummy packages each, with only the wirebond layer printed and with none of the metal package components brazed on. These dummy packages would be processed through gold plating using improved cutting,

punching and lamination techniques. Data relevant to ceramic particle contamination would be gathered, recorded and evaluated by Interamics and documented and reported to TI.

#### 6.1.3 Experimental Design

The experiments were designed primarily to identify the steps at which particulate contaminants were introduced, and secondarily, to evaluate the success of standard cleaning techniques.

Two groups of parts were processed, a control group and a test group. The test group was processed with a thorough cleaning before the particles were counted. The standard method for cleaning parts before firing is to carefully brush the part with a soft brush. The number of strokes of the brush is not a controlled variable, but the technique used is consistent. Parts in the control group were not brushed.

Both groups of parts were examined at five test gates. The number of particles present on the wire bond shelf area, which were greater than .002 inches across, were recorded at each gate. The first inspection was done immediately after circuit screening. The second inspection was performed after cavity punching. The third inspection was completed after lamination, and the fourth after the scoring operation. The fifth and final count was made after firing. A thin layer of electrolytic gold plating was applied to the parts before the final count to facilitate recognition of voids.

#### 6.1.4 Results

The average number of particles per part, at each of the gates, is plotted in Figure 101. The first bar in each group of two indicates the average number of particles counted without any brushing. The second bar indicates the average number counted on the parts which had been brushed.

The clear trend toward increasing numbers of particles in later processing steps indicates that each step adds more particulate contamination. The slight decrease between the post lamination inspection and the post scoring inspection for the unbrushed parts is not significant and is within the experimental error.

Finally, the large differences between the brushed and unbrushed conditions indicates the success which can be achieved by thorough brushing. The number of particles which remain after brushing may represent the practical limits of our present cleaning techniques.

#### 6.1.5 Conclusions

It is obvious from Figure 101 that brushing thoroughly after each step can drastically reduce the particulate surface contaminants which are larger than .002 inches. However, other conclusions drawn from this data may also prove insightful. The dramatic decrease in the number of particles present after firing may understate the damage which nonceramic particles can invoke. This final count did not include dents or impressions left by burned-out particles; it only includes actual particles which remain on the wire bond fingers. The fact that the number of unbrushed particles decreased by a factor of three



during firing, while the number of brushed particles decreased only by a factor of two, may indicate that brushing is slightly more effective at removing nonceramic particles than ceramic ones.

The largest increase in the number of particles per part appears to be from lamination. It is speculated that this increase is caused by the ceramic forming around the inserts during lamination and the subsequent removal of the inserts breaking off small pieces of ceramic. This possibility was considered during the work on lamination techniques and tools.

Figure 102 shows a photograph demonstrating the presence of particulate contamination and its effects. Figure 103 shows the reduction in particulate contamination which can be achieved by brushing.

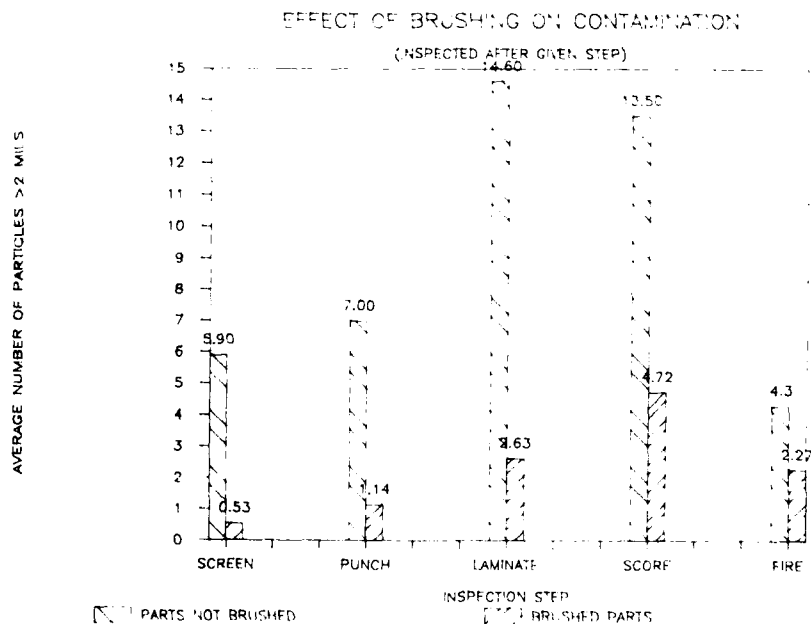


Figure 101. Brushed Sample.

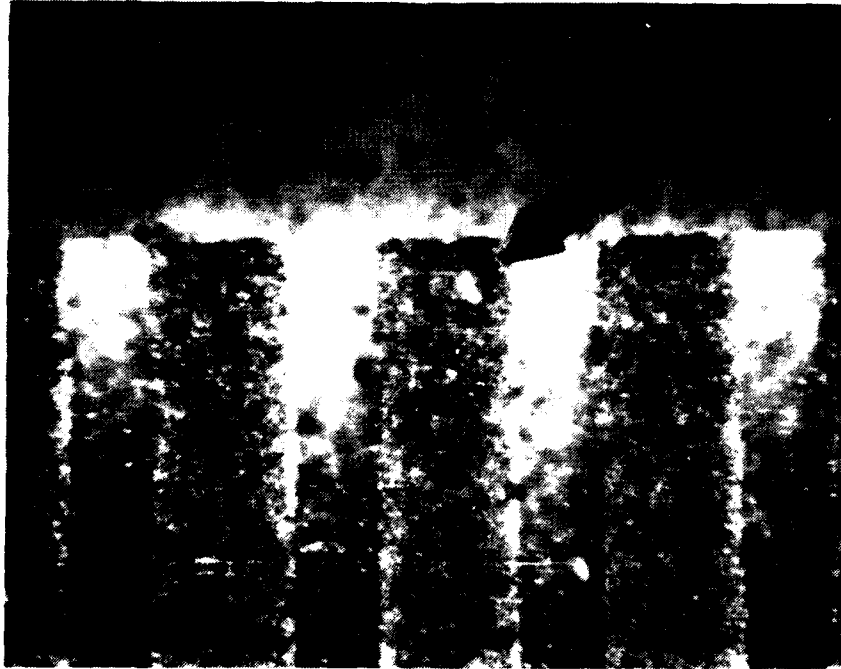


Figure 102. Void from Contaminant.

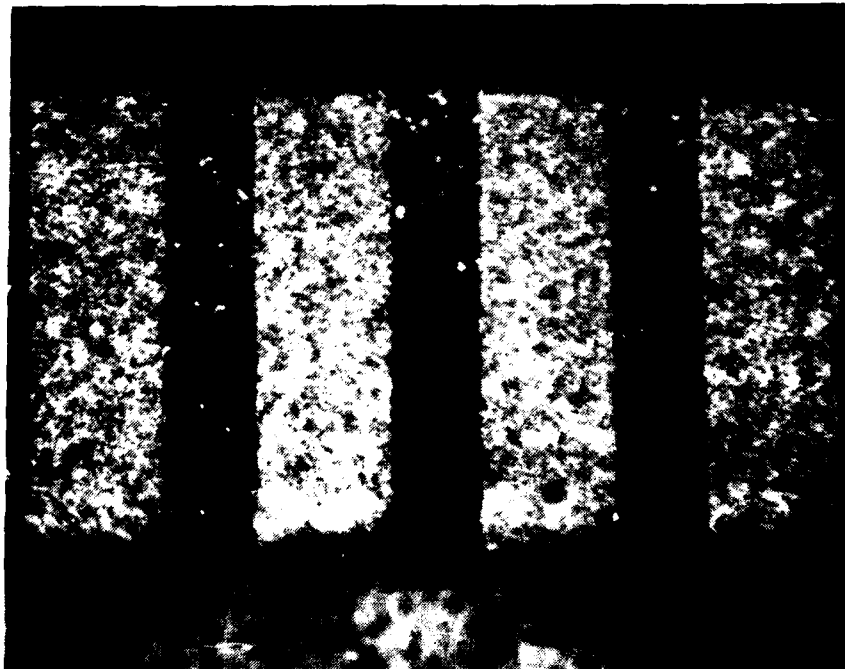


Figure 103. Particle Reduction from Brushing.

## 6.2 LAMINATION TECHNIQUES AND TOOLS

### 6.2.1 Statement of Problem

There were several problems associated with the lamination step of these products which were attributed directly to the lamination inserts used previously. Specifically, a slight gap between ceramic layers five and six was an indirect source of yield loss. This gap was not sufficient to be rejected as delamination, but it was large enough to trap plating solutions and lead to electrical shorting between adjacent wire bond fingers.

Another problem, a ridge or raised area which occurred in the capacitor cavities, was attributed to accumulated tolerances in the location of the capacitor cavity inserts. These inserts are very small and therefore difficult to handle. Occasionally, ridges were severe enough to warrant rejection of the parts and were unsightly. Most importantly, considerable time and effort were required by lamination operators to check the position of each small insert in an attempt to minimize this condition.

All inserts, even the newest and best designed ones, leave an impression where they are pressed into the ceramic. On these products, this impression was most noticeable on the wire bond fingers. While the flaw was not considered critical, it was cosmetically undesirable and could potentially interfere with wire bonding. Some parts have been lost because the impression was deep enough to cut through the metallization of the wire bond fingers, thus causing electrically open wire bond fingers.

### 6.2.2 Background

It was determined during Phase I that an increase in yields, production, lamination rates, and thereby, costs, could be achieved by the elimination of a possible delamination condition under the capacitor cavities. In order to accomplish this goal, a retooling of higher precision lamination inserts would be necessary. In this same area, various lamination techniques could be studied, evaluated and compared to determine the optimal lamination method. The baseline lamination rate established during Phase I of the contract was approximately three assemblies per hour.

Interamics proposed to start two lots of fifteen assemblies each to evaluate the effects of the proposed lamination process modifications. These dummy packages would be processed through firing with results documented and reported only to TI.

### 6.2.3 Experimental Plan

Three types of remedies were attempted for the problems identified above. The first, most direct approach was to modify or replace the tooling to eliminate the problems. New tooling was obtained, tested and evaluated.

The second approach was to design process steps which could fix the most undesirable condition. To this end, a dielectric screen was designed. Dielectric can be selectively screened onto the wire bond fingers under ceramic layer six. This thin insulating layer was intended to have two effects. First,

the dielectric would fill any gap which might occur, thus eliminating the possibility of trapping plating solutions. Second, the dielectric layer would insulate the wire bond fingers from any plated metal (gold), which might become trapped if a gap still existed. This method was also tested.

The third approach was to completely redesign the lamination process. The lamination technique which was originally used was based on the Interamics standard lamination process. The redesigned process, known as "tack lamination", does not use any inserts. It has been used successfully on a few special products. This process is not widely used at Interamics, because it is not the standard and because it requires additional processing steps, (i.e. each assembly is laminated as a series of subassemblies which are then "tacked" together).

#### 6.2.4 Results

The first approach, redesigned lamination inserts, resulted in a qualitative improvement in the product as shown in Figure 104. In particular, the new capacitor cavity inserts reduced the tendency of these small inserts to shift during lamination, thus reducing the ridges in the capacitor cavities. The gap between ceramic layers five and six also may be reduced somewhat. The depression in the wire bond fingers caused by the insert which supports the wire bond shelf also may have improved slightly.



Figure 104. Capacitor Cavity.

The screened-on dielectric appeared to be effective at filling any gaps between ceramic layers five and six. More importantly, screened-on dielectric eliminates the "gold bridging" between wire bond fingers which causes shorts.

The only drawback to the use of the dielectric is that it is slightly visible at the outside edge of the wire bond fingers as shown in Figure 105. A careful examination of these parts will reveal that the dielectric screen was not perfectly aligned to the cavity when these parts were fabricated. In other words, the width of the dielectric line is not exactly the same on all four sides of the cavity. A solution for this minor cosmetic distraction has already been devised but was not used in this study.

The completely redesigned lamination process, "tack lamination", has completely eliminated problems associated with the impressions left by lamination inserts as is evidenced in Figure 106. In addition, tack lamination seems to reduce the upward bowing of the ceramic in the capacitor cavity which can lead to voids between the ceramic and the heat sink after brazing. Furthermore, tack lamination reduces the visible symptoms caused by frequently seen misalignment of ceramic layers at the cavity wall.

The most disturbing aspect of the electrical shorts caused by plating solutions trapped in the gap between ceramic layers five and six was the difficulty in detecting it. Frequently, the gap was so slight it was not readily visible even at high magnification. The plating solutions do not become trapped until final plating (i.e. after testing for shorts), and are therefore not detectable by technical means. The net result is that a very careful final inspection is necessary under high magnification. This source of yield loss, along with the labor required to detect it, appears to be eliminated completely by screening on a thin line of dielectric. In spite of the added step this technique requires, it seems to be an extremely good method for preventing the "gold bridging" between wire bond fingers which causes electrical shorts difficult to detect.

Tack lamination appears to be a feasible process for these designs. It virtually eliminates most or all of the problems discussed above. The only drawback to tack lamination is that it increases the number of steps required for lamination, but it also eliminates the need for some other process steps. In balance, the total number of hours required to process a part through lamination remains roughly the same. However, the quality of the product is improved, and some improvement in yields is quite likely to be obtained. It is anticipated that any of these packages which are built in the future will employ both tack lamination and screened on dielectric. Figure 107 demonstrates this combined process.

Specific estimates of the percentage yield improvement resulting from this process improvement are not very significant because the tack lamination test sample size was comparatively small. However, among the test samples, no delaminations, no lamination insert imprints, and much less misalignment could be detected. In contrast, while there were no critical flaws in the group of parts made with inserts, varying degrees of the problems mentioned above could be detected easily.



Figure 105. Dielectric Exposure.

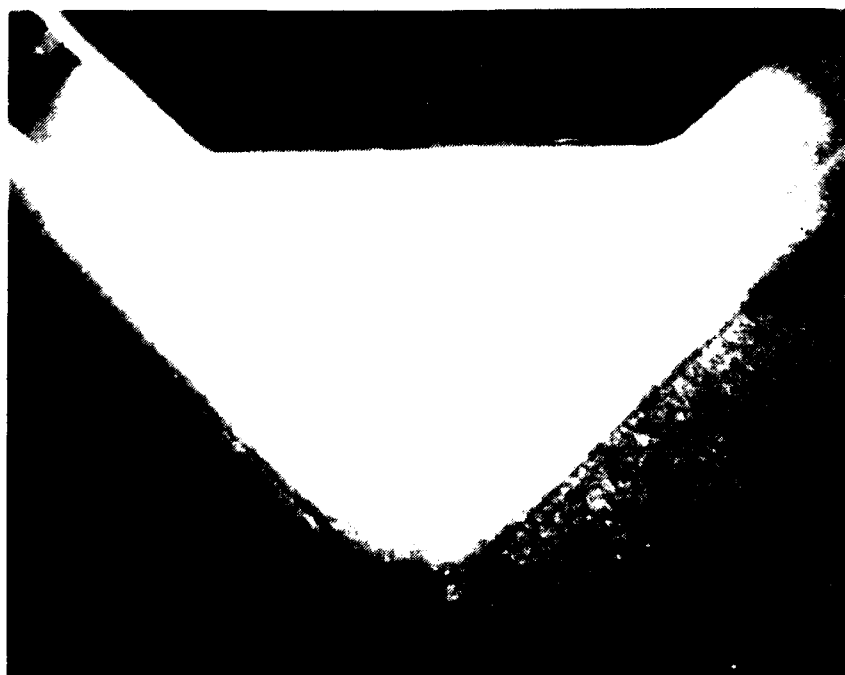


Figure 106. Tack Lamination.

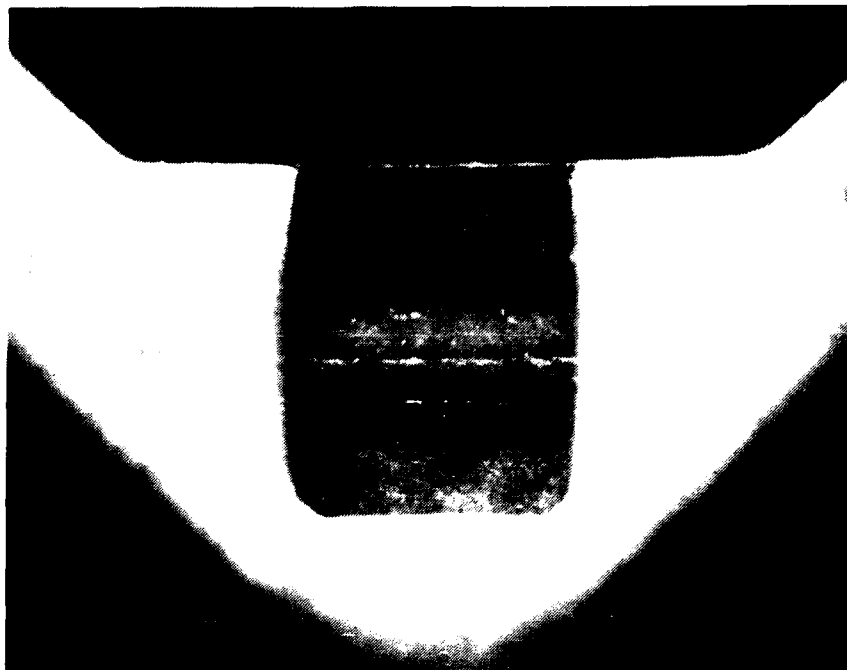


Figure 107. Tack Lamination/Screened Dielectric.

### 6.3 OPTIMIZATION OF FIRING RATE

#### 6.3.1 Statement of Problem

One of the factors affecting the cost of manufacturing these or any other ceramic parts is the amount of furnace space required to fire them. During the initial building of these designs, the unfired parts either were not trimmed or were only trimmed slightly before firing. Thus, they took up the maximum possible furnace space, which minimized throughput and maximized unit cost for the firing operation. This cautious approach was adopted because it was believed that unacceptable amounts of distortion would occur during firing if the thin ceramic frame of these designs was not adequately supported by the additional ceramic around the outside of the part. The intent of the firing rate optimization study was to determine an optimum size for the outside of the ceramic during firing. It was anticipated that the bowing of the cavities (the tendency of the square cavity to become round), would increase with decreasing firing dimensions. The 308 I/O design was selected for this study, because the bowing problem is most severe in this package.

#### 6.3.2 Background

Due to the "picture frame" style construction of the ceramic portion of the package, it was necessary for excess ceramic material outside the package perimeter to remain in place during processing to minimize distortion while firing. This action resulted in inefficient furnace loading since relatively

few of these large parts could be accommodated in a furnace during a single firing cycle. In order to lower package cost, a trade off study was proposed which would determine the optimum processing card size. This would result ultimately in a minimized part distortion while maximizing furnace loading.

One lot of fifty dummy assemblies was proposed for this effort. These parts would contain a few metallized layers to maintain realistic shrinkage characteristics. They would be cut to a range of different outside dimensions and fired. Distortion then could be measured and recorded after firing and evaluated as a function of the outside dimensions yielding an optimum card size. Results would be documented and reported to TI.

#### 6.3.3 Experimental Plan

A large group of dummy packages was divided into four groups before firing. Each group was scored (i.e. cut while in the unfired or "green" state), to a different size as follows:

- Group 1 - 4.5 inches square (uncut)
- Group 2 - 4.0 inches square
- Group 3 - 3.5 inches square
- Group 2 - 2.9 inches square (minimum possible size)

(Note that these are the green, or unfired, dimensions. Shrinkage of approximately 20 percent occurs during firing). Parts from these groups were mixed and randomly loaded into the batch furnace where they were fired in the standard manner.

After being subjected to a normal firing profile, the bowing of each side of each part was evaluated by measuring the distance between the edge of the cavity at the middle of the side and the (imaginary) line between the two adjacent corners. That is, the maximum curvature of each side of the cavity was measured. This measurement was plotted against the scored dimension of the sample.

#### 6.3.4 Results

Based on past experience, the anticipated amount of bowing was to be an inverse function of the scored size. However, the data does not support this expectation.

The first bar in each group of three in Figure 108 shows the average measured bowing as a function of size. There is no clear correlation. In fact, there is very little difference in the average amount of bowing which occurred.

The second bar in each group shows the range around the average measured bowing also as a function of scored size. This is quite clearly an inverse function of size. That is, the larger the scored size, the less variation there is in bowing.

The third bar in each group shows the standard deviation also decreasing with increasing scored size. This last data is primarily a consequence of the range decreasing with increasing size.



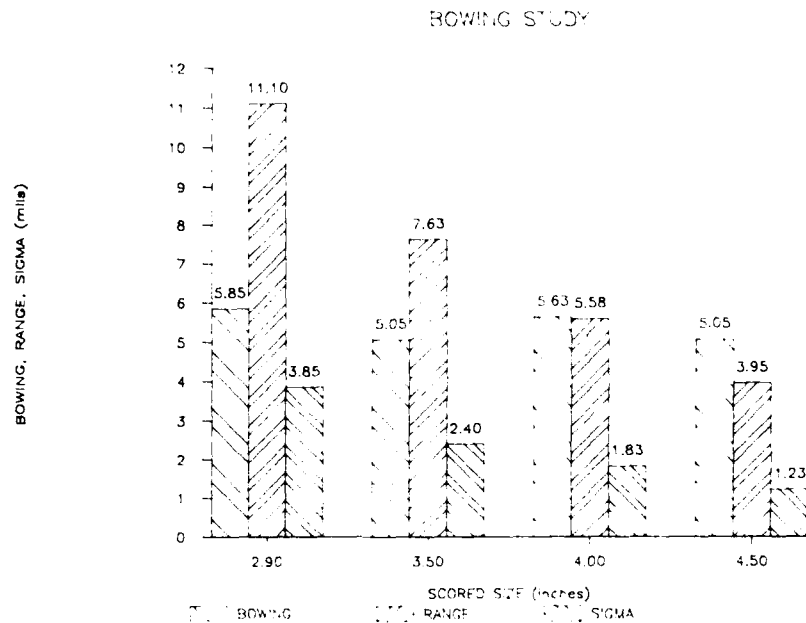


Figure 108. Firing Rate.

#### 6.3.5 Conclusions

At first glance, it appears that the bowing is not a function of scored size and therefore is a waste of furnace capacity to allow any extra ceramic around the outside of the parts during firing. This first impression is directly contrary to what was anticipated.

Upon closer examination, it is apparent that the amount of bowing is much more consistent and predictable when the scored size is larger. Assuming a standard (Gaussian) distribution, the data indicate a three sigma value of between .0085 inches and .0090 inches. That is, 99 percent of the sides of unscored parts should have less than 8.5 mils of bowing. Scoring even one quarter inch off of each side of a 4.5 inch square laminated assembly increases the three sigma value to around .011.

The primary impact of excessive bowing becomes apparent after brazing on lead frames. Leads which overhang the inside edge of the braze pads are the most common manifestation. Bowing also reduces the maximum shrinkage tolerance allowable for brazing purposes. Product yield losses due to incorrect shrinkage are the largest single source of loss on the 308 I/O design. Based on these findings, in the future Interamics will score very little, if any, ceramic off of the laminated substrates before firing. This choice is the one which was expected, but for completely different reasons.

## 6.4 SEAL RING TOOLING UPGRADE

### 6.4.1 Statement of Problem

The seal rings originally used for these products, were chemically etched. This process has the advantages of short lead time on initial orders and low initial tooling costs. The primary drawback of chemical etching is that it always causes some "undercutting" of the seal rings. The degree of undercutting is proportional to the thickness of the part being etched. Therefore, in order to remain within the specifications for the packages, .020 thick chemically etched seal rings had to be brazed together in a stack to achieve the required .040 seal ring height.

Handling of the .020 thick seal rings was difficult. They tended to bow, warp and bend if not treated with care. The additional brazing step required to join them together, added labor and material costs and increased the opportunity for damage. In addition, chemically etched seal rings sometimes had slight burrs which, though not severe, contributed to alignment and tooling difficulties.

### 6.4.2 Background

During Phase I, the seal ring of each of the two package designs was constructed using two .020 thick seal rings stacked and brazed together. This two layer construction allowed the use of chemically etched seal rings which are readily available and have a short lead time; however, the thickness of this type of seal ring is limited to .020 if undercutting tolerances are to be maintained. These thin seal rings then had to be stacked and brazed together to achieve the required overall height. An additional lapping step was required on occasion to ensure that the package thickness tolerance was met. To reduce labor, yield loss, assembly tooling and possible material costs, the seal ring ultimately should be fabricated as a single piece which can be brazed directly to the package body.

Interamics proposed to tool up the seal ring vendor so they could mechanically punch the .040 thick seal ring rather than chemically etch two thin rings.

### 6.4.3 Action

The tooling for fabricating stamped, .040 high, seal rings from a single piece of Kovar has been completed. The first samples received by Interamics did not consistently meet the specified flatness, especially on the 308 I/O design. The vendor identified the processing step which needed modification and has taken corrective action.

### 6.4.4 Results

The new .040 thick seal ring can be handled more easily than the chemically etched parts. There is much less risk of bending or bowing of the seal rings. The stamped seal rings which were inspected had no apparent burrs either.

The unit cost for the stamped seal rings, when ordered in small quantities, is not significantly lower than the unit cost of the equivalent etched parts. However, the quality is better and the amount of handling is reduced. Yield losses due to seal ring bowing should be reduced with the use of these rings.

## 6.5 SHRINKAGE CONTROL

### 6.5.1 Statement of Problem

The largest source of yield loss for the larger 308 I/O design is from lack of shrinkage control. The specifications for the ceramic portion of both package designs allow for 0.8 percent shrinkage tolerance. This tolerance is a standard design parameter for Interamics and results in acceptable yields. Unfortunately, in order to braze the lead frames onto these packages, much tighter tolerances must be held. Specifically, 0.3 percent shrinkage tolerance for the 308 I/O package and about 0.5 percent for the 196 I/O package are needed.

Chemical etching of the top layer pattern is one way in which the location of the braze pads can be assured. When this process is used, the shrinkage variability is less important. Theoretically, using chemical etching and 308 I/O substrates with shrinkage variations of up to 0.6 percent would still make good packages. Cumulative tolerating errors in the steps required for chemical etching may reduce acceptable shrinkage variation.

### 6.5.2 Background

The process which Interamics used in Phase I to produce the packages required that shrinkage be controlled to  $\pm 3$  percent of the total shrinkage. If shrinkage is normally 17 percent, then on any given lot it must be no greater than 20 percent and no less than 14 percent in order to maintain dimensional tolerances. Based on calculations involving the current geometry and location of vias, Interamics determined that it would be possible to loosen the shrinkage tolerance to  $\pm 5\%$  if a chemical etch technique could be used to create the top layer metal pattern. In addition to the direct increase in yields attributable to fewer size-related rejects, Interamics proposed that this method would have secondary beneficial effects on yields in the brazing operation. It would also possibly decrease handling time in brazing.

Interamics proposed to use an outside vendor for etching. This concept could be proven using dummy packages requiring only one layer to be via punched. Results of the study would be documented and reported to TI.

### 6.5.3 Experimental Plan

One test lot of dummies of each design were prepared with solid metallization on the top layer. A computer program was developed which, when used in conjunction with Interamics scribing saw, enables a partial compensation for uneven shrinkage within each part. Each design was sawed to a specified size with respect to center-line targets. This special sawing operation was required because two outside edges of the parts are used for locating during the imaging step of the chemical etch process.

The chemically etched parts would be examined for vias which are not covered by braze pads, measured, and evaluated for overall quality. The amount of shrinkage tolerance which is acceptable when the chemical etching process is used will be evaluated based on the results of these inspections.

### 6.5.4 Results

The chemical etching of the test lots has not yet been completed. Some technical issues were pending resolution with the vendor delaying tooling completion. It is believed that those issues have been resolved and delivery of the test lots should occur in the second quarter of 1988. After the parts are received by Interamics, evaluation will begin and an addendum to this report will be provided.

### 6.5.5 Conclusions

Chemical etching may provide a means to decrease the yield losses due to shrinkage variation, especially on the 308 I/O design. The potential yield increase which may be obtained by chemical etching has not yet been demonstrated for these designs. The primary concern is the cumulative effect of location errors in aligning, sawing, fixturing and imaging the parts before etching. Ultimately, the actual yields of this process must be weighed against the additional costs in order to determine cost effectiveness.

## 6.6 CONVERSION TO PRODUCTION TOOLING

### 6.6.1 Statement of Problem

Production tooling allows all of the holes needed in a piece of ceramic tape to be punched in one quick, highly repeatable operation. In addition to the reduction of labor, there are important secondary benefits. Interamics has a large number of machines (pneumatic presses) which can handle standard production tooling and a large number of operators trained in their use. Therefore, this step of the production process can be scheduled much more easily and completed quickly. Perhaps most importantly, using these tools leads to a more uniform product. Via locations are more repeatable and electrical yield losses are likely to be smaller.

#### 6.6.2 Background

The packages built by Interamics during Phase I of the VHSIC Multichip Packaging contract were built using prototype or "soft" tooling. Although it provides a shorter overall lead time on a first time order, the use of automated numerically controlled via punching equipment is labor intensive and creates a production bottleneck even for small orders.

Interamics proposed to build "one-up" hard tooling for each of seven layers on each of the two package designs. This was predicted to facilitate more rapid deliveries, lower labor costs, and increased yields.

#### 6.6.3 Action

Interamics has fabricated a complete set of production tools for each of the two designs. The tools have been inspected and tested. Samples of punched cards were previously provided to the program.

#### 6.6.4 Results

The most dramatic labor saving change made under the yield enhancement segment of the LABCOM Multichip Packaging program has been the conversion from "soft" prototype tooling to production tooling. The long term effects on yield is difficult to predict. The most direct benefits are the reduction in labor, increased capacity and ease of scheduling.

SECTION VII  
ELECTROMAGNETIC PULSE PROTECTION OF  
VHSIC DEVICES

7.0 INTRODUCTION

Electromagnetic pulse protection of VHSIC devices is a continuing packaging concern. This paper discusses EMP protection in general as it relates to high density microelectronics packaging of high speed devices. The paper in its entirety follows as section 7.1.

7.1 ELECTROMAGNETIC PULSE PROTECTION OF VLSI/VHSIC CHIPS

7.1.1 Introduction to EMP Effects

Electromagnetic pulse (EMP) protection of VLSI devices is required for continued operation in adverse operating environment(s). Packaging of devices to ensure operation after exposure to an EMP is complicated by the multiple effects of an EMP on various aspects of device and system performance.

This paper will discuss the impact of EMP and EMP countermeasures on VLSI packaging from the viewpoint of reducing the disruption that EMP can cause in system operation. It will not address device radiation hardening or impact of EMP on semiconductor device performance. These issues are relevant to the overall system survivability in an EMP environment and need to be considered in any overall system solution to EMP protection.

EMP will affect system performance in several different areas. Protection mechanisms that can be incorporated in packaging to minimize the impact of EMP will typically address only one aspect of the EMP disturbance, therefore a "layered" protection scheme must be used to minimize the overall impact of EMP. A partial listing of the means by which EMP can impact system performance follows.

1. All effects are associated with induced currents and voltages that exceed design expectations or device limitations. The EMP effect is seen as an induced voltage or current on conductive materials within the electronic assemblies, and in particular, within the interconnect structures.
2. The location (insertion point) of the induced voltages and currents indicate the type of problem that will result. For example, on device-to-device interconnect, voltage spikes may falsely trigger digital inputs. On power supply lines, excessive power may be applied to devices. On ground and power planes within the interconnect structure, induced effects may result in abnormal circuit operation.
3. In addition to electronic disruption, physical damage is also possible. EMP induced voltages can result in a corona discharge which ruptures interconnect dielectric materials, causing either short or open circuit conditions. Excessive current pulses can exceed the current carrying capacity of conductors and cause material meltdown resulting in open and short circuit conditions.

### 7.1.2 Worst Case EMP Scenario

The magnitude of EMP surges on a specific device is proportional to the length of the conduction path (interconnect) and the orientation of conductor(s) to the radiated EMP field. For a typical scenario, a 50 Megaton high altitude (100km) blast, the induced EMP field at ground level is estimated at 50,000 volts/meter [1]. This induced EMP can be modeled as a step impulse with 10 ns duration.

For a SMT PWA, we will consider the case of a typical worst case length interconnection of 10 inches, with a conductive interconnect 8 mils wide parallel to the EMP source and an inductance (L) of 200 nH/meter.

Using a first order approximation of:

$$I = 2 \times C/L \times dV/dT \text{ where } C \text{ is interconnect area constant} \\ (10 \text{ in} \times 8 \text{ mils} = .038 = C)$$

for the instantaneous current surge averaged over a nominal 10 ns duration interval of an EMP, the induced current on the interconnect due to the EMP would be:

$$I = 2.5E7 \times .038 \times 12.5E3 \times 10E-9 = 120 \text{ amps} \\ \text{C/L(H) voltage over time} \\ \text{interconnect area}$$

The current can be modeled as a modified Gaussian pulse with a -3 dB point occurring 5 ns after the current peak magnitude. The overall energy associated with this transient current is:

$$W = 2 \times I^2 \times L/C = 0.0303 \text{ joules}$$

### 7.1.3 Options in Management of Package Level EMP Suppression

Three methods for managing effects of EMP within the domain of package and PWA level packaging will be discussed. They are the following:

1. Electronic device protection using commonly employed circuit design techniques, such as insertion of voltage and current limiting components/designs and available components to minimize the impact of EMP on a packaged device by attenuating the EMP at the package I/O.
2. Assembly level shielding and PWA level EMP reduction techniques in the design process of the PWA to control and limit the buildup of EMP induced charge on the overall PWA.
3. PWA optical interconnect approaches that provide a high level of EMP immunity due to lack of electromagnetic interaction with the EMP energies. Optical, as opposed to conductive, interconnect has several advantages for use with electronic assemblies, but the technology with regard to intraboard interconnects and packaging is still immature and unproven.

These three methods for dealing with EMP protection of electronics are not mutually exclusive; to reduce the overall impact of EMP a combined approach may be optimal. In "layering" different types of EMP countermeasures the overall immunity of the system can be improved and degradation due to EMP artifacts is minimized. Each of the proposed methods for management of EMP effects are discussed in detail in the following sections.

#### 7.1.4 Electronic Protection Measures for Attenuation of EMP at Package I/O

Conventional, proven approaches to package and device level noise reduction may be utilized to minimize the impact of EMP on device and system performance. These EMP suppression techniques include:

The inclusion of power suppression and filtering components either added or integrated into package I/O barrier(s) of all devices. These types of components may include:

1. Zener diodes or other voltage sensitive (ie. spark gap, surge arrestors) components used to protect solid state devices from excessive voltages from an EMP. Due to the fast turn-on needed to catch the EMP surge (<5 ns), low capacitance Zener diode techniques are needed to be able to respond properly.
2. Low pass filtering components may be used to attenuate the high frequency components of an EMP. Filter configurations such as L and Pi section filters with series inductance and shunt capacitance can either be inserted into the package I/O or built into the signal pad or pin.

Power pins, due to the large areas associated with power planes and power supply interconnects are especially susceptible to noise and power surge generation of an EMP pulse. The types of voltage suppression and filtering described above are critical for package power pins in order to prevent current surges and over voltages that may damage the device.

Use of opto-couplers at package I/O provides a high degree of isolation between the interconnect and device inputs. Since an opto-coupler uses a light emitting transmitting / light sensitive receiver pair to provide data interface, high voltage and other electromagnetic artifacts are isolated from the device, providing a high degree of EMP protection. There are device related problems related to use of opto-couplers at VLSI speeds and with EMP power densities such as:

1. Opto-coupler switching speeds must be  $\geq 100$  MHz to prevent degradation of VLSI/VHSIC signal integrity/fidelity. These bandwidths may permit EMP generated noise and artifacts to be passed into the device and will isolate the power components of the EMP.
2. The opto-coupler must have EMP pulse power dissipation features to ensure that the opto device itself does not burn out due to the EMP surge.



3. Opto-couplers are essentially one way devices; VLSI I/O is often bi-directional. Bi-directional isolation and coupling must be supported for use with traditional bus systems. Development of device and circuit technology and manufacture should be oriented toward optimal insertion of opto-couplers in high density, complex designs.

Large area low impedance grounding is needed to minimize inductively generated EMP currents and noise buildup and insure that adequate discharge paths exist within the package for the EMP. High power dissipation and high speed grounding techniques such as the grounded thermal via approach TI Patent Pending [3] as used on VHSIC-1 LCC packages may be appropriate. Anti-static materials to prevent voltage buildup within packages also are required to provide protection from EMP artifacts.

#### 7.1.5 PWA Level and EMP Control

Damage to electronic devices from EMP artifacts are typically due to large charge buildups on a PWA area perpendicular to the source of the EMP surge. Minimalization of this charge buildup can reduce damage and malfunctions to electronic systems in an EMP environment. Methods for minimizing EMP charge buildup in systems can include:

1. Application of conductive coatings to the PWA to isolate devices from the EMP sources. Grounded conductive coatings over insulating layers of protective material can provide a means of draining off charge buildups before damaging levels are reached.
2. Since the worst case EMP surge is a high altitude blast, orientation of PWAs to minimize the board area exposed to EMP source (i.e. mounting all PWAs vertically as opposed to horizontally) may reduce charge buildup.

#### 7.1.6 Geometrical CAD Design for EMP Control

High voltage buildup on PWAs can result in an energy discharge phenomenon occurring at angular discontinuities of a conductor (package or interconnect). If an energy concentration is not discharged into system ground adequately, voltage levels can occur that may ionize an air path into the nearest ground plane. This energy discharge can cause damage, including burning of package or PWA due to the high energy discharge into package or PWA ground planes.

This phenomenon known as "corona effort" may be averted by elimination of angular discontinuities (i.e. square pads, 30, 45, 60, 90° turns) in conductor path(s) in the package and overall PWA interconnect. Package and PWA level drafting and CAD procedures and tools to insure rounded pads and graduated curves in interconnect may prevent corona discharges within the PWA and package environment.

#### 7.1.7 Package Level Optical Interconnect for EMP Suppression

Optically based interconnect technologies have inherent advantages over conventional conductor based VLSI interconnects in terms of electromagnetic isolation and resistance to EMP surge artifacts. These advantages include:

1. Resistance to electromagnetic coupling of noise
2. High rejection ratios to power supply variations
3. Inherent high resistance to EMP generated artifacts
4. High bandwidth allowing signal multiplexing.

Intraboard optical interconnect technology is relatively immature. Although integrated optical wave guides have been demonstrated in the laboratory as early as 1973, high tolerances and exotic materials required for successful and repeatable procedures have limited application of optical interconnects. Among the major issues that need to be addressed for optical interconnects to be utilized in a PWA environment for EMP suppression are:

1. Manufacturable methods of embedding or depositing optical transmission materials onto PWB substrates. Radically different methods from current organic and ceramic substrate technologies may be required to support optical interconnects. Current processes can be assumed to be inadequate in supporting manufacture of optical intra-PWA interconnects.
2. Optical IC technology and manufacture development oriented toward the goal of creating inexpensive, low power devices that are compatible with intra-package integration with digital logic. Current approaches to optical IC packaging and integration place a prohibitively high overhead on a system in terms of power and density to be used in more than protection of a few critical signals.
3. Optical multiplexing of busses and other design techniques to optimize use of optical interconnects. Optical interconnect hardware typically is expensive and complex due to high tolerances required for low loss interconnects.
4. Low cost, low insertion loss optical interfaces and connectors are required to allow optically interconnected devices to be inserted, removed and replaced from substrates. Connectors must be small enough to be compatible with high density PWA design methodologies as well as be able to efficiently couple optical signal information.
5. Electro-optical receivers and emitters capable of handling the high throughput and the quantity of signals typical in a high density signal processing PWA while maintaining a low enough power and board area ratio is not to be a major overhead item in the PWA design.

Traditionally optical interconnects have been used in high speed transmission of data over long distances where complexities can be justified. For optical interconnects to be successfully employed in the PWA packaging environment, significant amounts of development are needed to insure that optical interconnection technologies are competitive in meeting performance as well as EMP protection criteria.

#### 7.1.8 Recommended EMP Packaging Development Activities

Texas Instruments supports the concept of working to implement and EMP suppression capability into current generation packaging technologies. The following list of development activities are based on the preliminary research for this report and are recommended as initial steps to define and develop the required packaging technologies for inserting a "layered" EMP suppression capability into conventional military PWA assemblies.

1. Develop and evaluate integrated filter, Zener, and opto-coupler design approaches for insertion into package I/O for electronic protection.
  - Evaluate both high speed and good transient power performance of Zener and opto-coupler devices
  - Develop suppression circuit design, optimization, insertion and test techniques compatible with high density packaging
2. Develop and evaluate current conductive coatings as well as the coating and insulation techniques for both package and PWA EMP protection.
  - Develop conductive coating procedures directly insertable into current military products coating specifications
3. Develop CAD post-processing capability to minimize/eliminate angular discontinuities in both package and PWA layout and design.
  - Develop generic algorithms and CAD system specific implementation
4. Evaluate and recommend best approach to implementing optical interconnect technologies for intraboard suppression of EMP.
  - Detailed system level analysis of optical interconnect options
  - Evaluate current technology approaches to integration of optical interconnects for military PWAs in preparation for the next phase development of optical interconnect capabilities

These efforts will provide a near term, staggered approach to generating an EMP suppression capability for intra-PWA and package development. A second follow-up effort to the optical interconnect study phase for development of optical interconnect technologies such as connectorless optical package to PWA interconnects, optical receiver/transmitter devices and optical wave guides and light pipes would be a logical and natural extension to this effort. Development efforts of this type would also be highly compatible with other (i.e. high speed) packaging and interconnect technology thrusts, where optical interconnect approaches are expected to be required.

#### 7.1.9 Bibliography

- [1] "Protecting Electronic Equipment Against EMP Effects" New Electronics, July 1987.
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- [3] "Grounded Thermal Pad for VLSI/VHSIC Packaging" Submitted TI Patent Disclosure (N. Stollon / J. Hatcher / L. Derryberry) Docket #TI-11955.
- [4] "Integrated Optics Mirror Microwave Concepts" Microwaves, May 1975  
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## SECTION VIII

### LABCOM MULTICHIP PACKAGING TEST REPORT

#### 8.0 INTRODUCTION

According to contractual agreement between Texas Instruments and the U.S. Army LABCOM, testing was done to evaluate and demonstrate the performance of the SRAM, both the package and its interconnect as a whole. This report summarizes the parametric and functional test results of the X4 SRAM LABCOM VHSIC Multichip module.

The report is divided into three sections: Test fixture design/approach, Test results and Conclusion.

#### 8.1 TEST FIXTURE DESIGN/APPROACH

In Phase I, the LABCOM module was tested using the Fairchild Sentry 21 supported by Texas Instruments GEFE (Government Electronics Front End). Due to the limited production line capability of the Sentry, the Pacific Western System COLT III tester was introduced to provide high volume testing of the 8Kx9 SRAM. Since GEFE is no longer supporting the SRAM on the Sentry, fixture changes were required for testing the LABCOM module.

A new custom test fixture, shown in Figure 109, was built to interface with the COLT III. The fixture design concept was evolved around fast clock pulse testing for the SRAM. Controlled characteristic impedance cables were implemented to provide matched impedance with the tester. Also, cables were kept as short as possible to eliminate line inductance and capacitance.

To make electrical connections between the package and the tester, a 196 I/O socket manufactured by 3M/Textool was utilized. First, the X4 SRAM module was mounted in a carrier, then placed inside the socket and oriented upside down so that the bottom of the package faced upward for improved heat convection during testing.

The COLT III test configuration for the X4 SRAM module was very similar to the Sentry 21 test configuration. Figure 110, depicts the schematic of the module. For testing purposes, all addresses (A0-A12), control data lines (CT)-CT\_), protection violation (PV\_), clock/write enable (CLK/WE\_), and data bus lines (DQ0-DQ8) were bussed together externally, but each SRAM has an independent chip select line (CS\_) for selecting purposes.

Figure 111, shows the wiring diagram of the 196 I/O socket interfacing with the COLT III I/O connectors. OR-gates (54AS32) were used as buffers for selecting and deselecting the X4 SRAM. By switching S1, each internal SRAM can be tested independently. By-pass capacitors were also used to decouple high frequency components and noises.

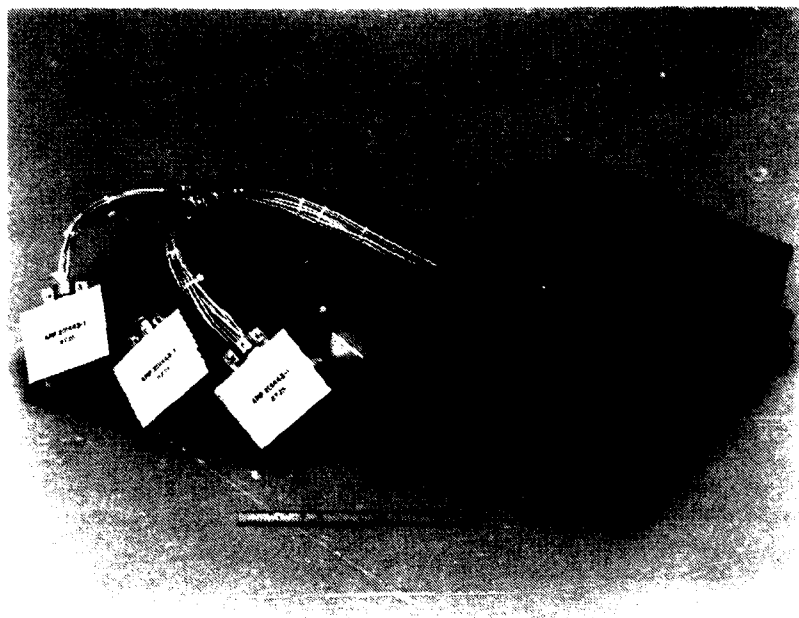


Figure 109. LABCOM X4 SRAM COLT III Interface Test Fixture.

## 8.2 TEST RESULTS

With the existing production test software for the 8Kx9 SRAM, minor modifications were required to accommodate the current consumption of the X4 SRAM module. Difficulty was encountered due to the limited supply current of the tester. In dynamic mode, the module was drawing the maximum output current of the 3.3V power supply (200mA). Due to this difficulty, the module was tested only at its nominal voltages ( $V_{cc}=5.0V$  and  $V_{dd}=3.3V$ ).

Appendix G describes the detailed design for the computer software programs identified as Colt III Test Programs for the VHSIC 72K SRAM device.

Appendix H and I show the DC and AC parametric test results of the X4 SRAM module. Note that each SRAM was tested independently for functionality in both pipelined (synchronous) and non-pipelined (asynchronous) modes. Also the main and auxiliary memories (control RAM) were separately tested. Cycle timing values were measured and compared against the specifications and the results are shown in Table 26 below.

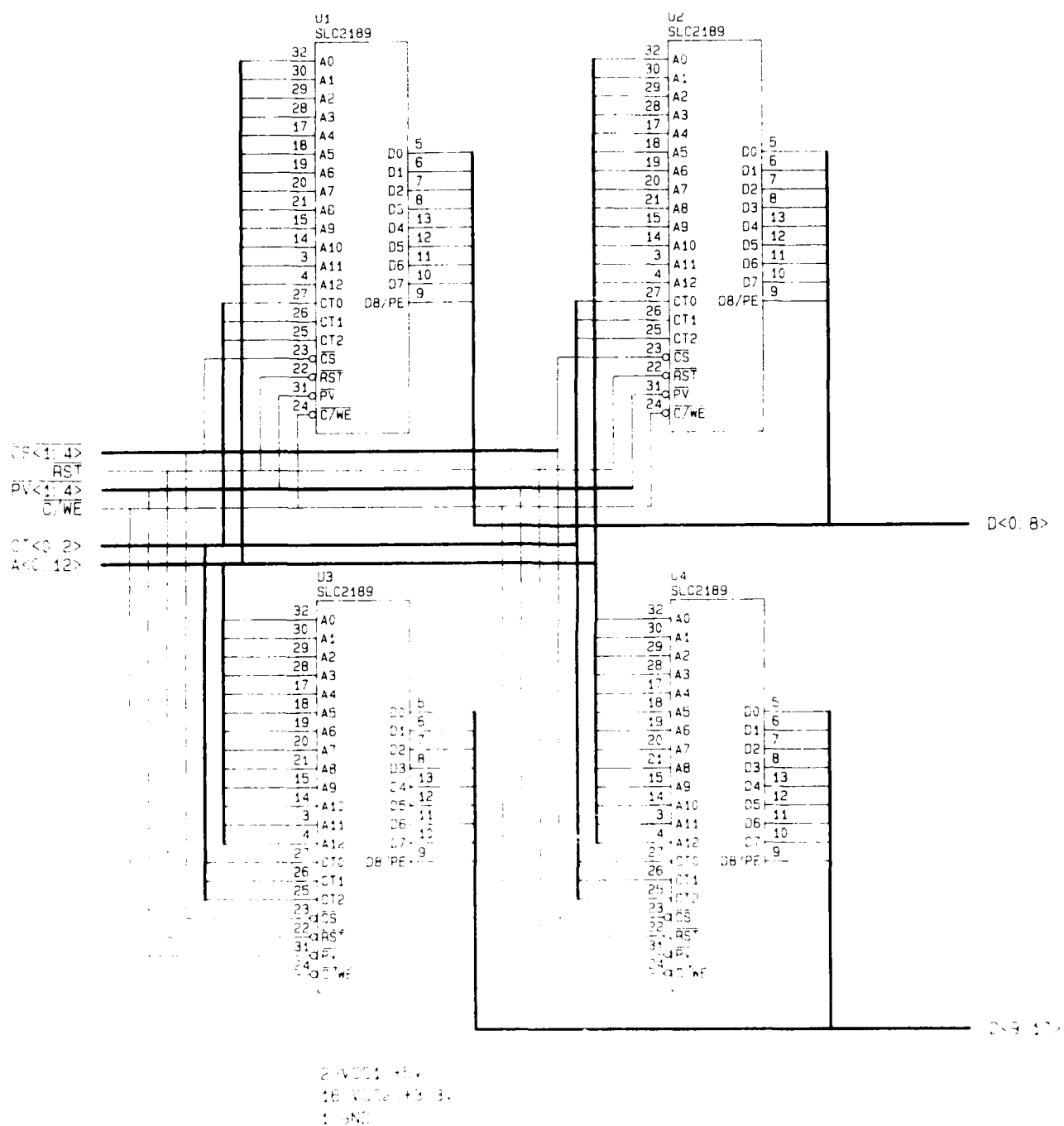


Figure 110. LABCOM VHSIC Multichip X4 SRAM Schematic.

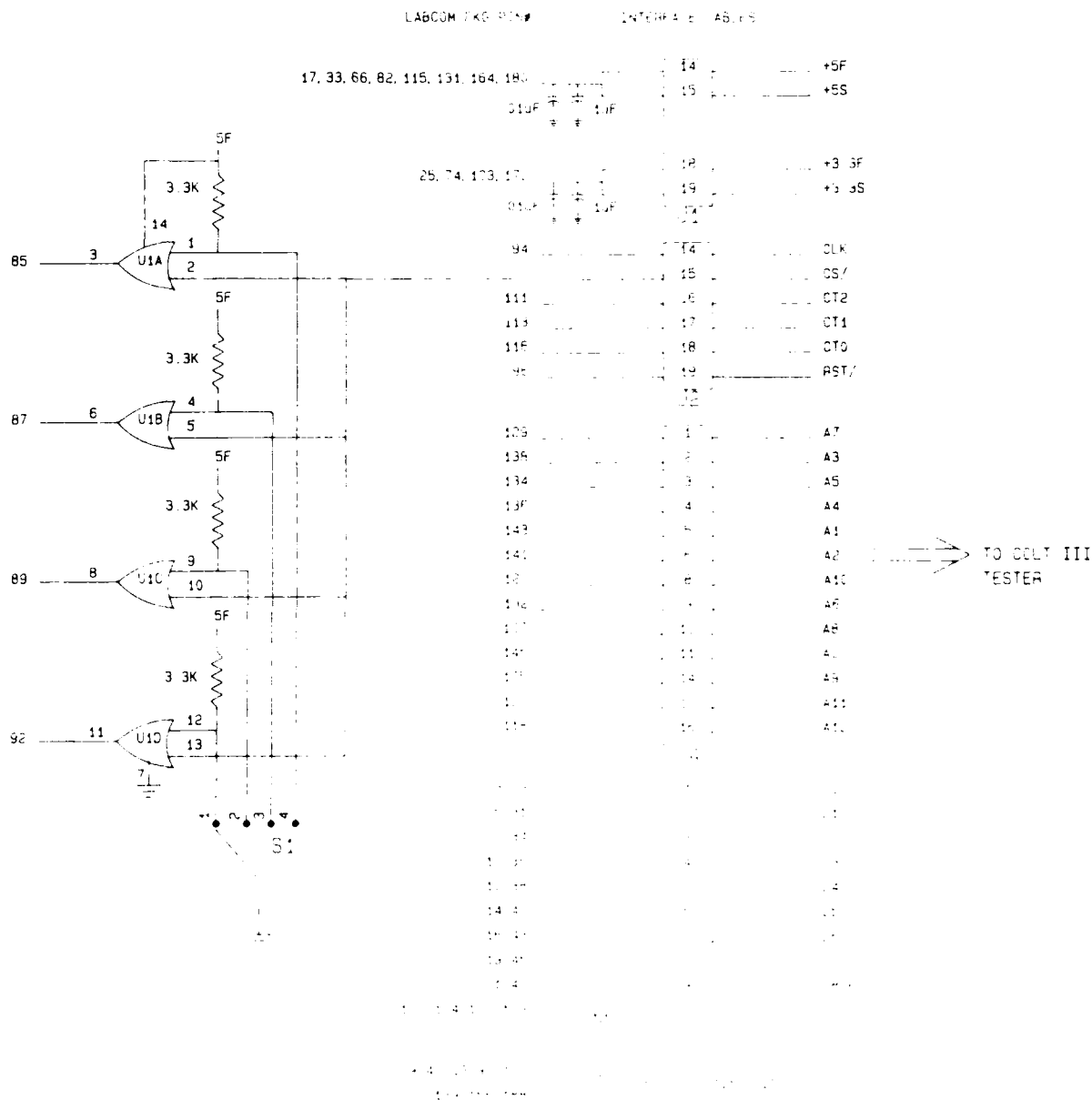




Table 26. Main Memory Timing Cycle Measurements

MODE/PARAMETER	SPECIFICATIONS	MEASURED			
		SRAM #1	SRAM #2	SRAM #3	SRAM #4
1. Non-pipelined					
(Read cycle)					
a. Tdacs (ns)	43	47.3	46.3	44.3	43.5
b. Tdaa (ns)	45	45.5	43.8	917.0	42.5
c. Tdz (ns)	18	24.0	24.8	22.5	22.3
(Write cycle)					
d. Tds (ns)	13	19.8	19.3	20.5	19.3
e. Twp (ns)	14	21.3	21.8	92.3	21.3
f. Tah (ns)	0	-17.8	-17.8	35.5	-17.0
2. Pipelined					
(Read cycle)					
a. Tdc (ns)	40	49.8	44.8	46.5	43.3
b. Tasuc (ns)	7	15.5	15.5	13.8	13.3
c. Tdhc (ns)	4	13.0	13.5	13.0	13.5
(Write cycle)					
d. Tdsuc (ns)	13	17.8	17.3	17.8	17.3
e. Tdhw (ns)	0	-4.0	-3.8	-3.8	-3.8
f. Twpc (ns)	22	28.3	29.0	27.0	27.0

- NOTES: 1. Only main memory test cycle timing is specified above.  
 2. Specification values are typical values listed in Appendix J  
 3. See Appendix J for explanations of above abbreviations.  
 4. Negative timing specifies that held time is not required.  
 5. Discrepancy of SRAM #3 was due to data line failure.  
 6. Each SRAM was tested independently.  
 7. Tests were performed at +25C with Vcc=+5.0V and Vdd 3-3V.

The most significant parameter of the SRAM is the access time which determines how fast the data can be stored and retrieved from the memory. Appendix G shows that the main memory read access times, Tdacs and Tdc, of all four chips varied from 43.5ns to 47.25ns in non-pipelined mode, and from 32.25ns to 24.35ns in pipelined mode respectively. The typical values, per the specification sheet in Appendix J, are 40ns and 43ns for pipelined and non-pipelined modes respectively. (note that the typical values were tested and recorded from the 32 pin LCC package SRAM).

Input and output package currents were measured and are given in Appendix I. Since all four SRAMs have common address lines, data bus, and control lines, the measured currents are the total gate package currents of the module with four SRAMs in parallel. Chip select (CS<sub>0</sub>) current is the input package current of the 54AS32.

Standby and active currents of the module were also observed. Table 27 shows the measured and calculated currents of the +5V and +3.3V supplies. Notice that the measured values are in the expected range.

Table 27. LABCOM X4 SRAM Module Power Consumption.

MODE	CALCULATED	MEASURED	TOTAL POWER
1. Standby			
a. 3.3V	4x15mA = 60mA	75mA	3.3Vx75mA = .25mW
b. 5.0V	4x6mA = 24mA	26mA	5.0Vx26mA = .13mW
			Total = .38mW
2. Dynamic			
a. 3.3V	3x15 + 1x140 = 185mA	195mA	3.3Vx195mA = .64mW
b. 5.0V	4x6mA = 24mA	27mA	5.0Vx27mA = .14mW
			Total = .78mW

- NOTES: 1. Calculated total current is based on the typical vlaues given in Appendix I.
2. In the dynamic mode, one SRAM is active and the rest are standby.
3. 54AS32s current is excluded from this Table.

Although 100 percent functional test was performed, only three of the four SRAMs passed the bit check. Failure occurred when SRAM #3 was tested. Preliminary troubleshooting and analysis showed that D3 of SRAM #3 failed to respond. Therefore, tests were performed with D3 masked out and this masking only affected the non-pipelined and pipelined main memory tests. This means that the control memory of the SRAM #3 is fully functional and passed 100 percent bit check. Also, with this masking only 88 percent of the total 72K main memory of the SRAM #3 was 100 percent checked.

Electrical contact was another difficulty encountered during testing of the module. Because of the high density I/O lead of the package, the carrier must be forced down to the socket pin during testing to make good contact. Due to this problem, temperature testing of the module was omitted.

### 8.3 TEST CONCLUSION

Additional testing provided Texas Instruments useful electrical information on parameters on the 196 I/O package, interconnect, and the SRAMs as a whole. Although many difficulties occurred during testing, especially when the SRAM #3 data line failed to respond, the overall test results show that the X4 SRAM module has performed well, as expected.

## SECTION IX OVERALL CONCLUSIONS

Overall, the LABCOM VHSIC Multichip Packaging program has demonstrated the high speed and density packaging concept and technology. New fabricating processes and testing were developed and addressed throughout the program. In general, the TAB technology has provided TI with the leading edge of testing I.C.s prior to packaging. Full static and dynamic electrical screening now can be performed prior to mounting the I.C. thus improving the overall yield of the final hybrid module. The TAB strategy also supports full range temperature testing including pre-seal burn-in as required. The pre-seal burn-in can be easily performed to screen out any infant mortality or early lifetime failures. In addition, a high speed and high power interconnect substrate was implemented and fabricated. High I/O pin count testing concepts were also demonstrated. Electrical and thermal modeling and characterization of the package were important issues which have been addressed.

The LABCOM VHSIC Multichip Packaging program has provided Texas Instruments with the opportunity to demonstrate and develop in-house testing and fabricating process which will benefit both Texas Instruments and future customers.

The execution of the LABCOM Multichip Packaging contract has resulted in the execution of the following items:

- A survey of Phase I VHSIC contractors that analyzed the perceived packaging needs of newly developed VHSIC IC's
- The design and development of a 196 lead fine-pitched package suitable for mounting 2-4 interconnected VHSIC IC's
- The design and development of a 308 lead fine-pitched package suitable for mounting 5-9 interconnected VHSIC IC's
- Development of a series of processes and tools required to fabricate the packages and interconnects
- Development of a United States owned and operated facility for manufacturing the 196 and 308 lead packages
- A complete analysis of the 196 lead package electrical characteristics (RF and Power)
- Design, encapsulation, and full functional test of a useful circuit incorporating VHSIC devices
- Implementation of TAB processing on VHSIC SRAM's
- Development of fine-pitch socketing for the 308 package
- The design and development of a 4-chip module consisting of four SRAMs, a thick film substrate, and a 196 I/O package
- Development of a source for a 196 and 308 I/O package and parts are now available from Interamics, Inc., San Diego, California.

APPENDIX A  
ASSEMBLY WORK ORDERS

<u>Page</u>	<u>Drawing Number</u>	<u>Document</u>
A-2 - A-5	2437701	Assembly Work Order (Wafer Processing)
A-6 - A-8	2437702	Assembly Work Order (TAB Processing)
A-9 - A-11	2437703	Assembly Work Order (Module Processing)

SH 1

[illegible]

ASSEMBLY WORK ORDER

LABCOM MULTICHIP PROGRAM

WAFER PROCESSING

[illegible]

74 88838


DWG NO 2437701 SH 2

ASSEMBLY WORK ORDER  
LABCOM MULTICHIP PROGRAM  
WAFER PROCESSING

PART NUMBER	WAFER LOT/WAFER NUMBER
	/

PAGE 1 OF 2

OPERATION	LOCATION	DESCRIPTION	DOCUMENT	DATE	OPERATOR
10	HDIL	WAFER INSPECTION	AI-02		
20	HDIL	METALLIZATION	SP-102		
30	HDIL	PHOTORESIST	SP-104		
40	HDIL	EXPOSE AND DEVELOP	SP-105		
50	HDIL	INSPECT PHOTORESIST	AI-05		
60	HDIL	GOLD BUMP PLATING	SP-106		
70	HDIL	PHOTORESIST STRIP (TOP)	SP-108		
80	HDIL	PHOTORESIST (BACKSIDE)	SP-104		
90	HDIL	GOLD ETCH	SP-110		
100	HDIL	TIW ETCH	SP-112		

 <b>TEXAS INSTRUMENTS</b> <small>Dallas, Texas</small>	OWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		A	96214	2437701	
SCALE			SHEET		2	

2437701

SM 3

LABCOM MULTICHIP PROGRAM

## WAFER PROCESSING

PART NUMBER : WAFER LOT/WAFER NUMBER

PAGE 2 OF 2

OPERATION	LOCATION	DESCRIPTION	DOCUMENT	DATE	OPERATOR

110 : HDIL : WAFER MOUNT : SP 116 : :

120	:	HDIL	:	WAFER DICE	:	SP-118	:		:
-----	---	------	---	------------	---	--------	---	--	---

130	:	HDIL	:	INSPECT DICED BAR	:	AI-11	:	:
-----	---	------	---	-------------------	---	-------	---	---



DWN	DATE
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SIZE	FSCM NO
<b>A</b>	<b>96214</b>

DRAWING NO  
2437701

REV

ISSUE DATE

SCALE


SHEET 3

### TRouble SHEET

LABCOM MULTICHIP PROGRAM

PART NUMBER	WAFER LOT/WAFER NO	DIE NO	MODULE NO

[illegible]

 <b>TEXAS</b> <b>INSTRUMENTS</b> <small>Dallas Texas</small>	DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		A	96214	2437701	
			SCALE		SHEET	4



[illegible]

ASSEMBLY WORK ORDER  
LABCOM MULTICHIP PROGRAM  
TAB PROCESSING

PART NUMBER : DIE NUMBER

PAGE 1 OF 1

[illegible]

210 : HDIL : INNER LEAD BONDING

: SF-202

220 : HDIL : IL BOND INSPECTION

: AI-12

230 : HDIL : ISOLATION

1 SF-

240 : SOUTH BLDG : ELECTRICAL TEST

DWG

(SINGLE CHIF TAB)

XXXXXXXXXX



DWN	DATE
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SIZE	FSCM NO
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**A 96214**

DRAWING NO

2437702

REV

ISSUE DATE

SCALE

SHEET

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DRAWING NO

2437702

SH 3

## TROUBLE SHEET

## LABCOM MULTICHIP PROGRAM

PART NUMBER : WAFER LOT/WAFER NO : DIE NO : MODULE NO

DATE : OPERATION : DESCRIPTION : ACTION TAKEN : OPERATOR



DWN

DATE

SIZE

FSCM NO

A

96214

DRAWING NO

2437702

REV

ISSUE DATE

SCALE

SHEET

3

[illegible]

DWG NO

SH

## ASSEMBLY WORK ORDER

## LABCOM MULTICHIP PROGRAM

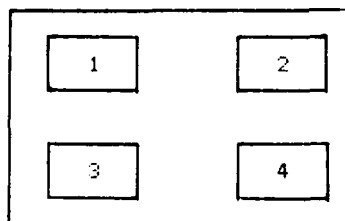
## MODULE/PACKAGE PROCESSING

PART NUMBER : MODULE NUMBER  
2437686 :

PAGE 1 OF 2

MODULE NO SRAM 1 SRAM 2 SRAM 3 SRAM 4

/ / / /



OPERATION : LOCATION : DESCRIPTION : DOCUMENT : DATE : OPERATOR

310 : HDIL : EXCISE : SP-204 : : :

320 : HDIL : DIE MOUNT : : : :

330 : HDIL : OUTER LEAD BONDING : SP-206 : : :

340 : HDIL : OL BOND INSPECTION : AI-14 : : :

350 : SOUTH BLDG : ELECTRICAL TEST : DWG : : :

: (X4 INTERCONNECT MODULE) : 2437693 : : :



DWN DATE

SIZE FSCM NO

A 96214

DRAWING NO 2437703

REV

ISSUE DATE

SCALE

SHEET 2

DWG NO

SH

## ASSEMBLY WORK ORDER

LABCOM MULTICHIP PROGRAM

MODULE/PACKAGE PROCESSING

PART NUMBER : MODULE NUMBER  
2437686 :

PAGE 2 OF 2

OPERATION	LOCATION	DESCRIPTION	DOCUMENT	DATE	OPERATOR
360	PEL	SUBSTRATE MOUNT			
370	PEL	WIRE BONDING	SP-11340		
380	PEL	WIRE BOND INSPECTION	MIL-STD		
			883/2001		
385	PEL	BOND STRENGTH			
390	SOUTH BLDG	ELECTRICAL TEST	DWG		
		(PRE SEAL PACKAGE)	2437694		
400	HDIL	LID SEAL	SP-208		
410	HDIL	VIS/MECH INSPECTION	AI-15		
420	SOUTH BLDG	ELECTRICAL TEST	DWG		
		(POST SEAL PACKAGE)	2437694		

 **TEXAS**  
**INSTRUMENTS**  
Dallas, Texas

DWN DATE

ISSUE DATE

SIZE FSCM NO

**A 96214**

SCALE

DRAWING NO

2437703

REV

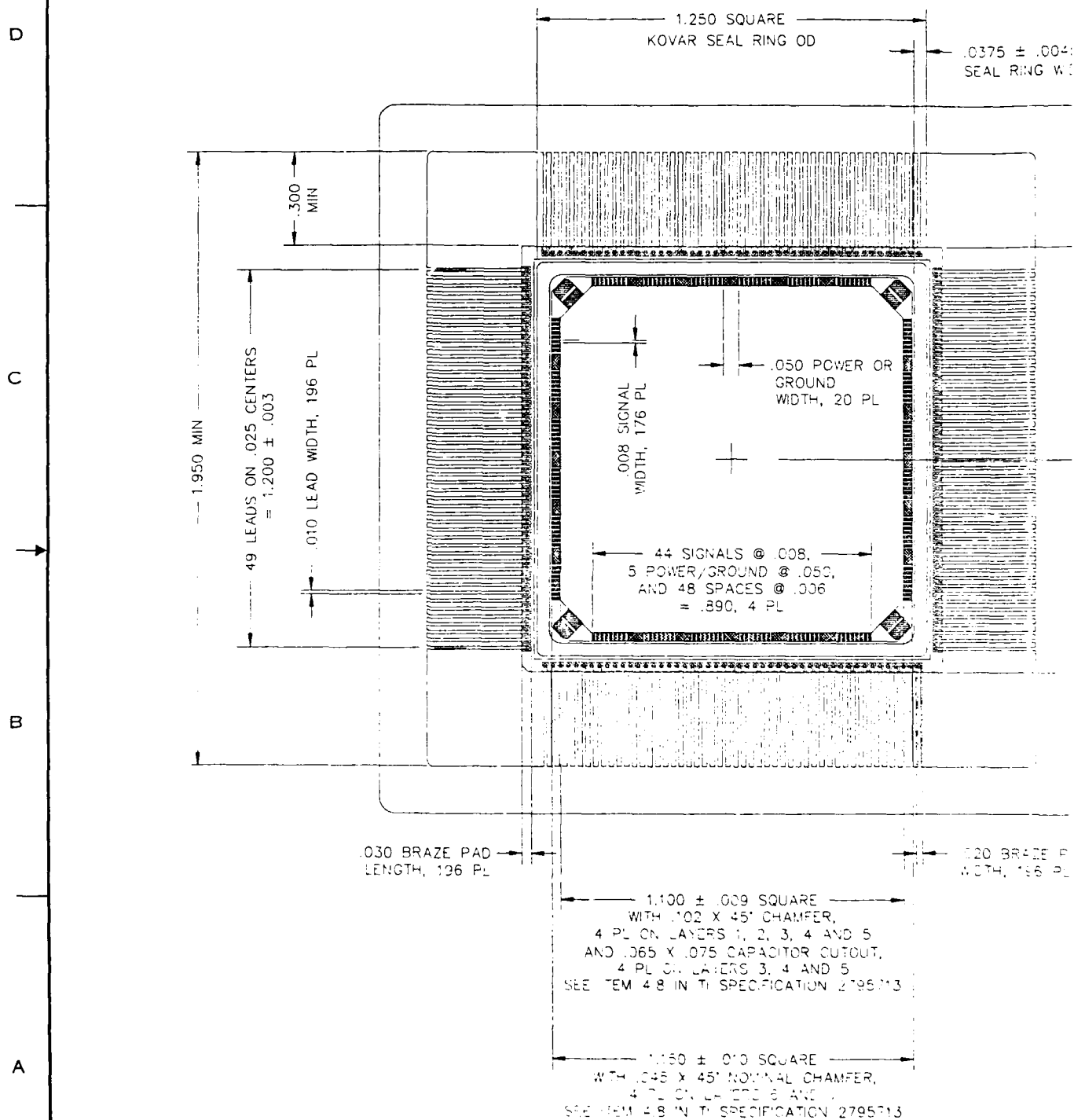
SHEET 3

APPENDIX B  
MECHANICAL DRAWINGS

<u>Page</u>	<u>Drawing Number</u>	<u>Document</u>
B-2 - B-3	2795724	196-lead Package
B-4	78-8056-9271-8	196-lead Socket (Carrier, Quad Pack 196 Lead)
B-5	2XX-6583-00	196-lead Socket ("Quad-L" Chip Carrier Socket)
B-6 - B-7	2795722	308-lead Package
B-8	2437705	308-lead Socket Drawing
B-9	2437706	308-lead Carrier
B-10 - B-19	2795713	General Package Specification
B-20 - B-25	2795712	308 Socket Specification
B-26 - B-34	2891091	Header Lid, Stepped
B-35	2437704	Loading Fixture
B-36 - B-42	2686134	Lead Form and Clip Tool

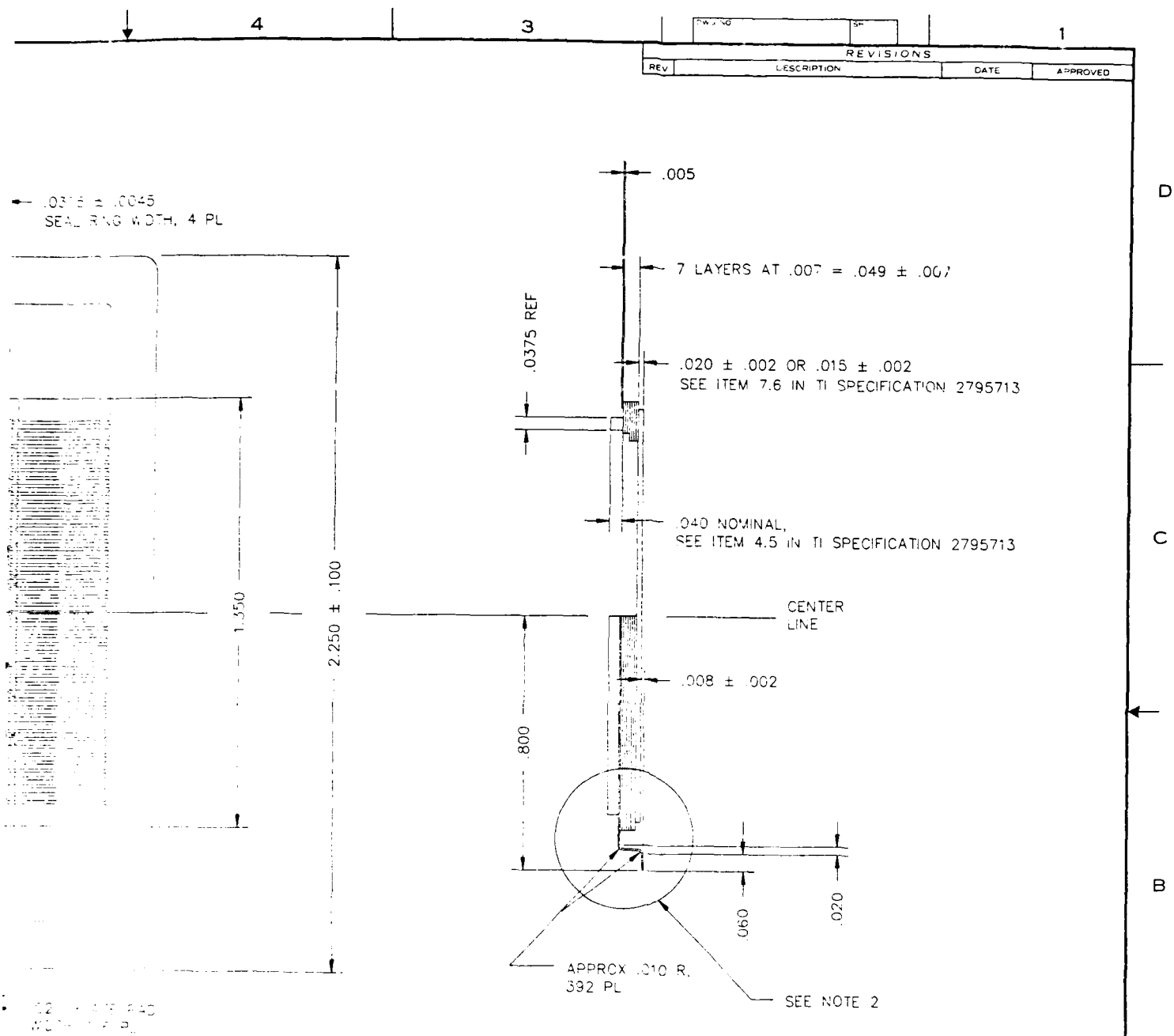
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2. AREA WITHIN CIRCLE SHOWS LEAD FORMATION AFTER FORMING AND CLIPPING.

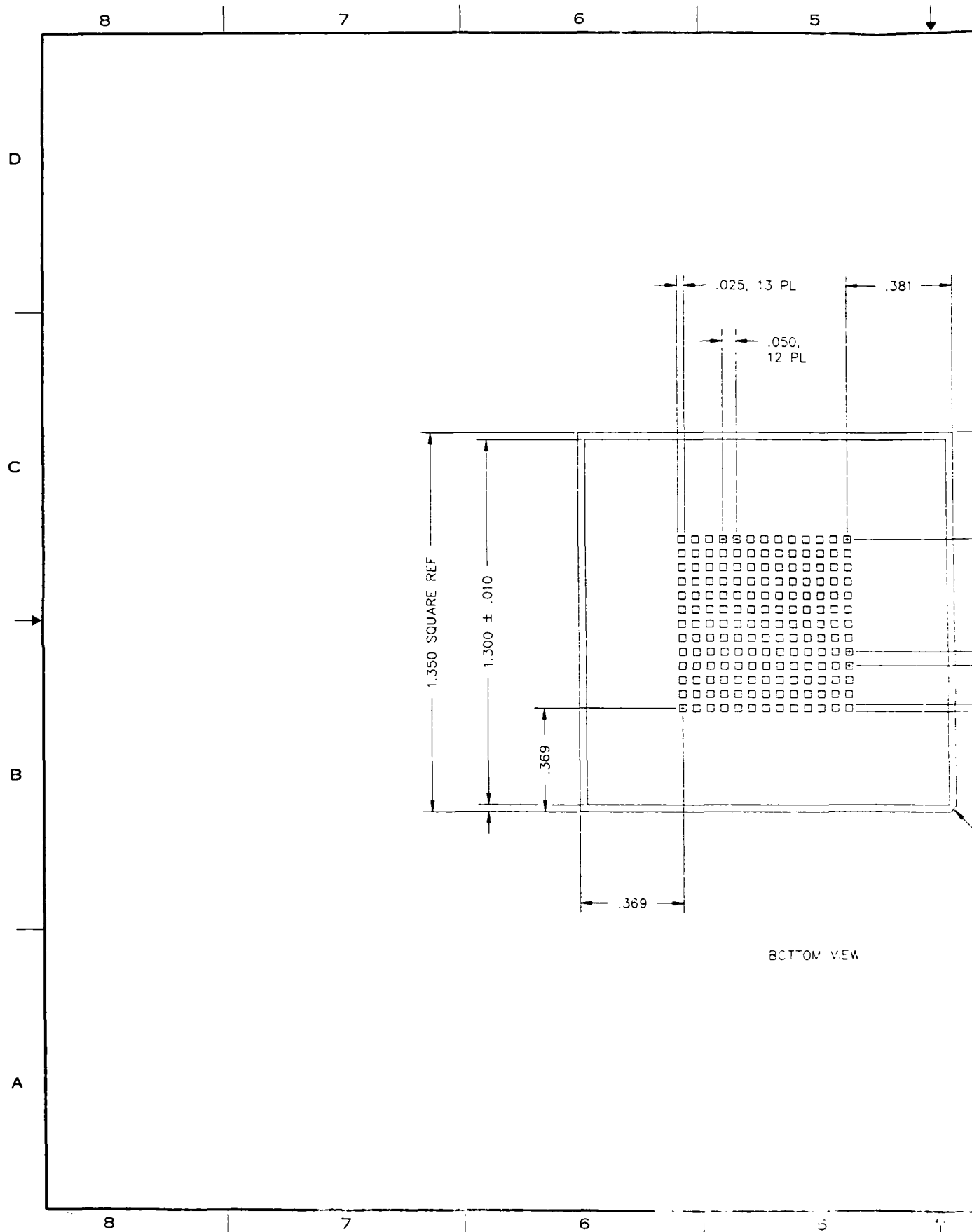


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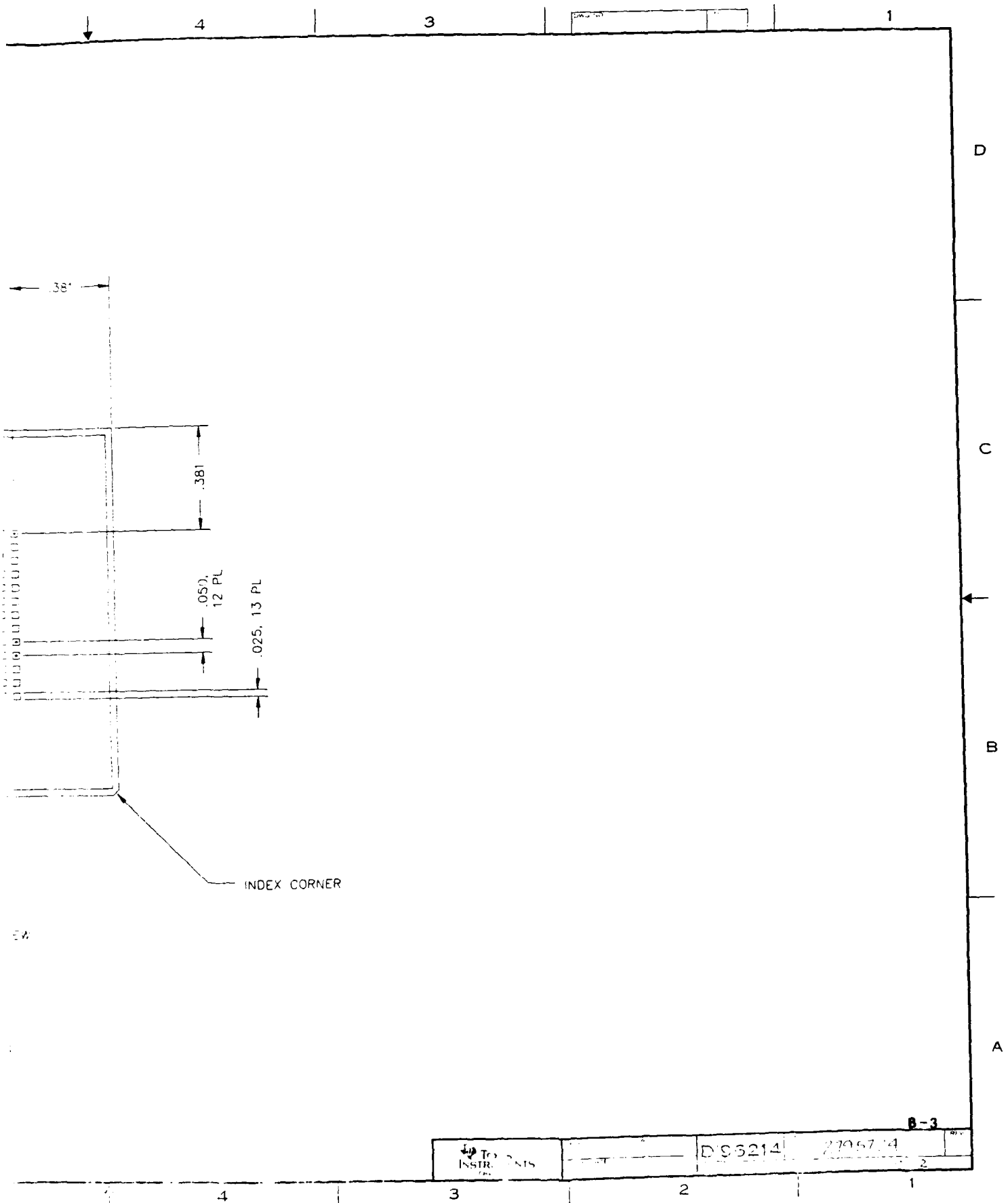


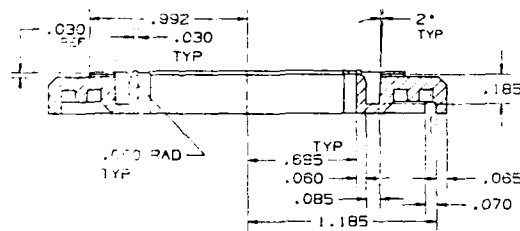
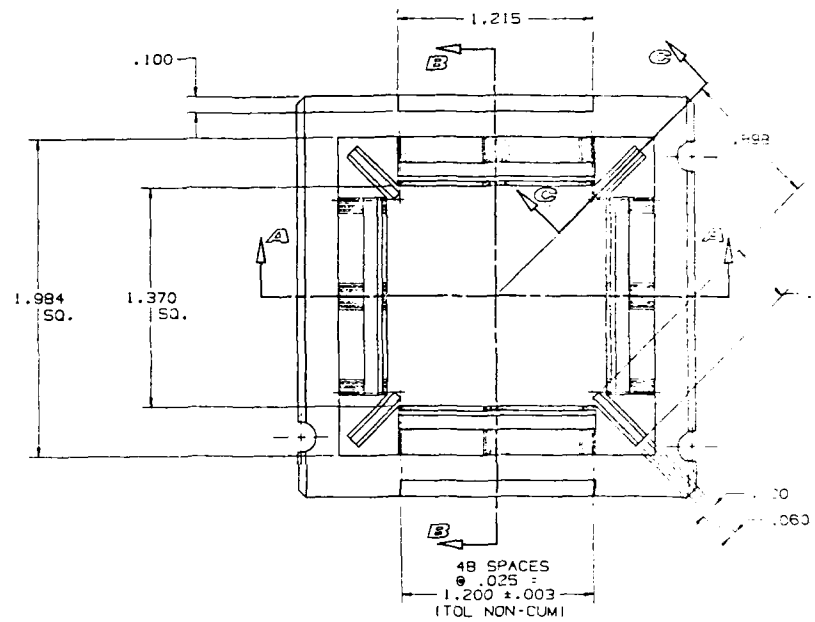


1		2		3		4																	
REV	DESCRIPTION	DATE	APPROVED	REV	DESCRIPTION	DATE	APPROVED																
PART OR IDENTIFYING NUMBER				NOMENCLATURE OR DESCRIPTION																			
PARTS LIST				PARTS LIST																			
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125	125	125	125	125	125	125	125																
<p>TEXAS INSTRUMENTS</p> <p>CHIP CARRIER, 196 LEAD, LARGOON VMC</p> <p>D 96214 2795724</p>				<p>0E2</p>																			

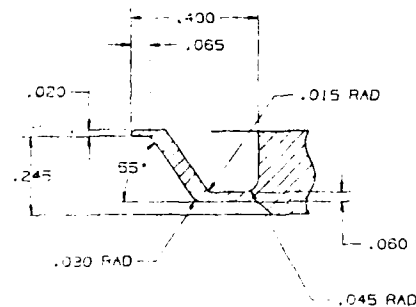


BOTTOM VIEW

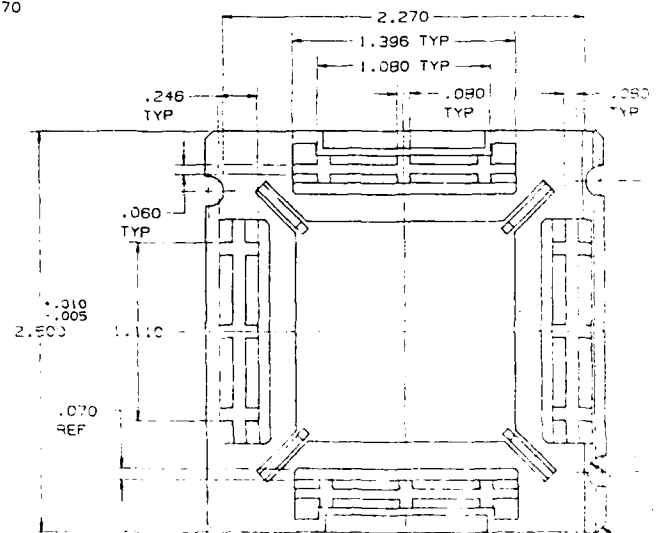




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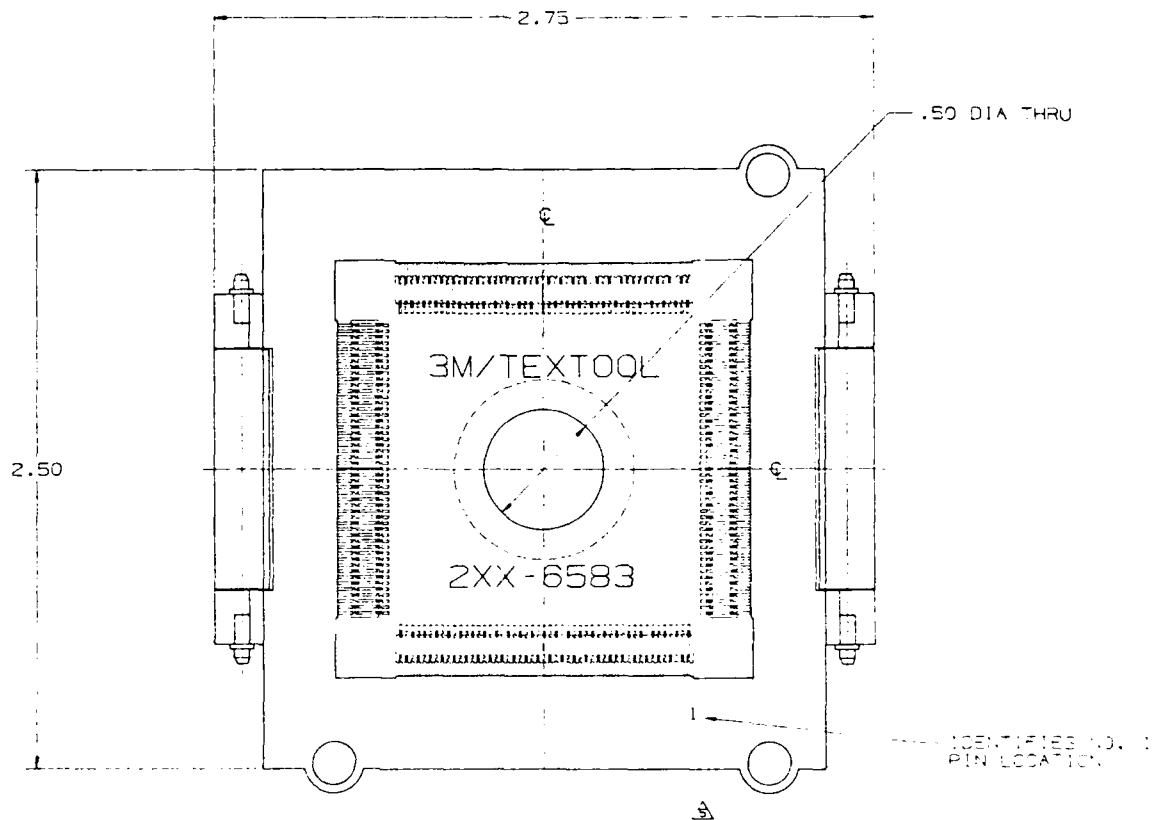


DETAIL "C-C"  
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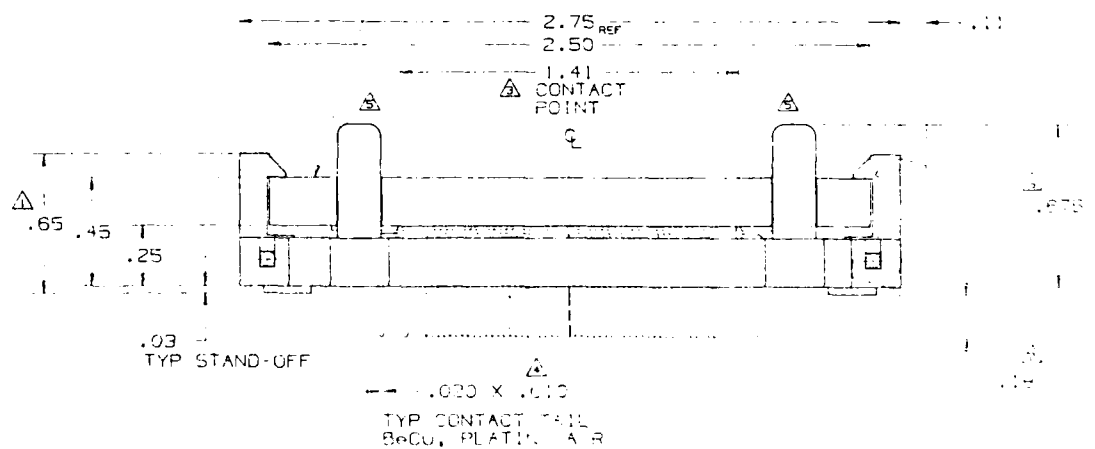


1.010  
1.045





CARRIER NOT SHOWN  
IN TOP VIEW



1.300  
SQ.  
48 EQ. 5PCS.  
⑨ .025±.002  
TOL. NON ACCUM.  
(4 PLC)

C

.025  
REF.

100 TYP

1.374  
SQ.

1. MATERIAL: 30% G.F. POLYPHEYLENE SULFIDE
2. FINISH: MOLDED
3. UNLESS OTHERWISE NOTED DIMENSIONS ARE SYMMETRICAL ABOUT CENTERLINE WITHIN A .004 WIDE ZONE

REF ID: A66585

CONFIDENTIAL

		B-5	
R	6.70	△ UPDATED POST CROMETRY	DSP
A	1.70	△ .010 WAS .008	DSP
		△ 1.41 WAS 1.40	
		△ .19 WAS .09	
		△ .65 WAS .58	
		RE-DRAIN	DSP

[illegible]

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NOTES: UNLESS OTHERWISE SPECIFIED:

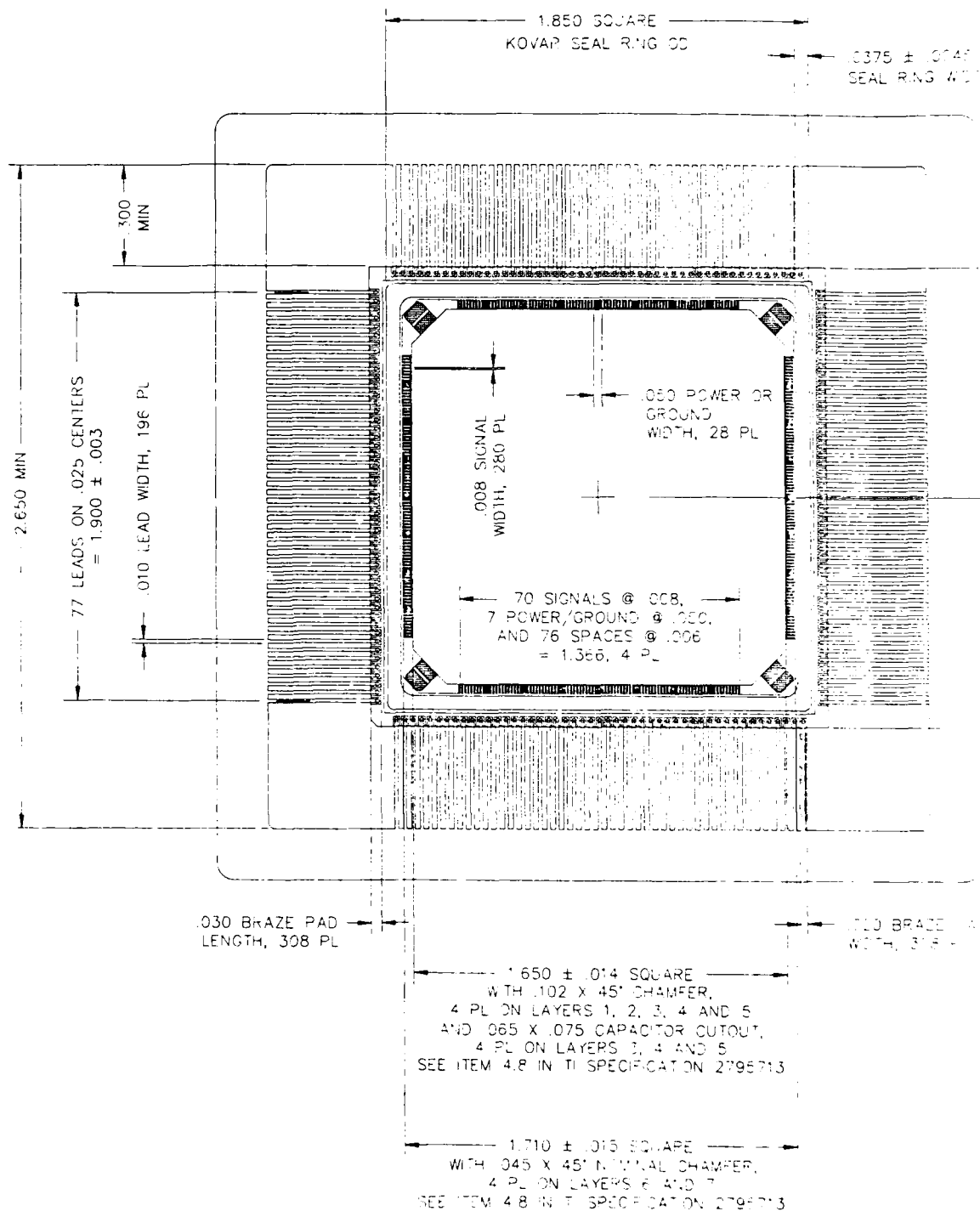
1. THIS PACKAGE SHALL BE FABRICATED IN ACCORDANCE WITH TI SPECIFICATION 2795713
2. AREA WITHIN CIRCLE SHOWS LEAD FORMATION AFTER FORMING AND CLIPPING.

D

C

B

A



REV	DATE	BY	CHKD	APPROVED	DESCRIPTION	QUANTITY	REMARKS
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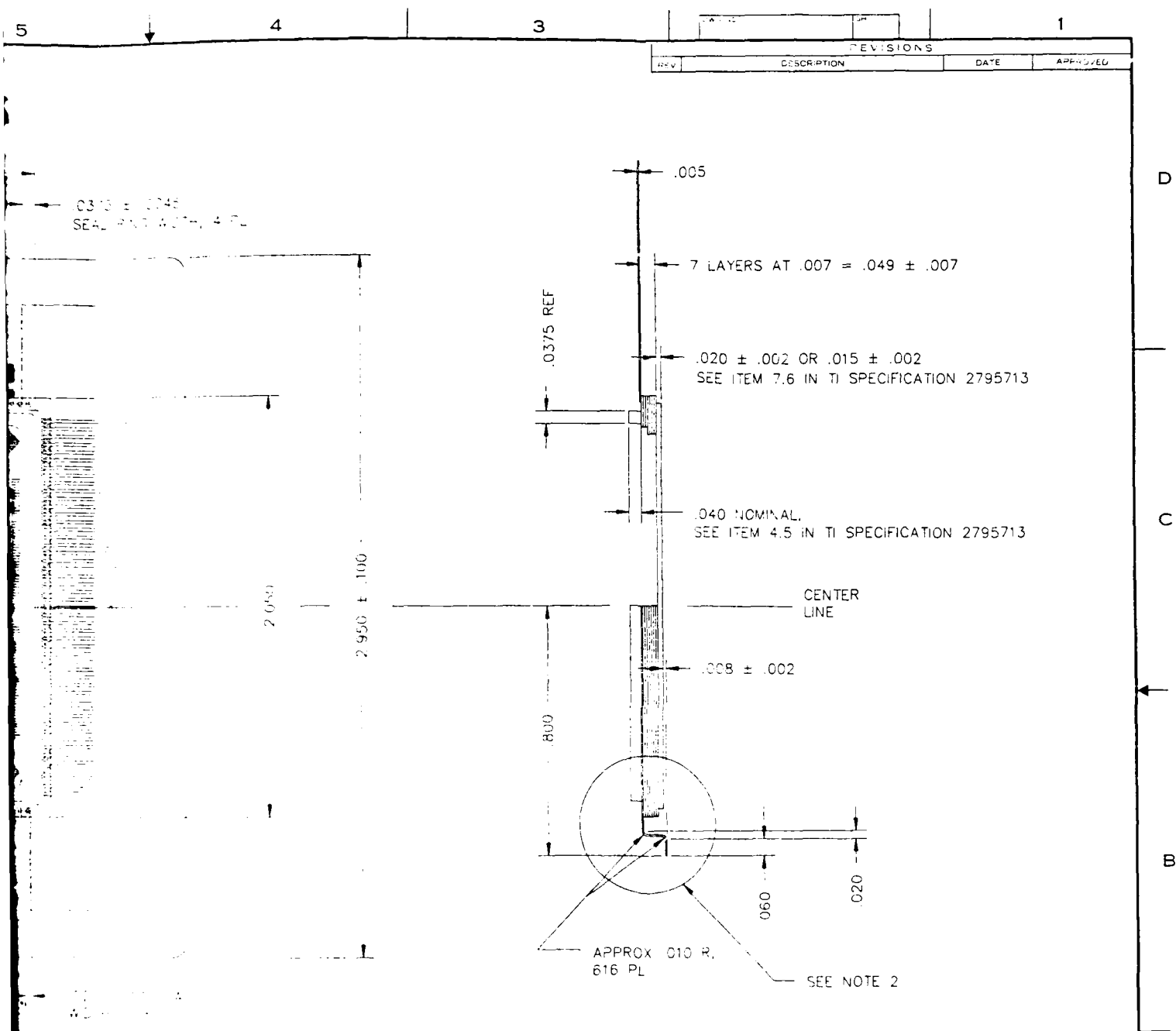
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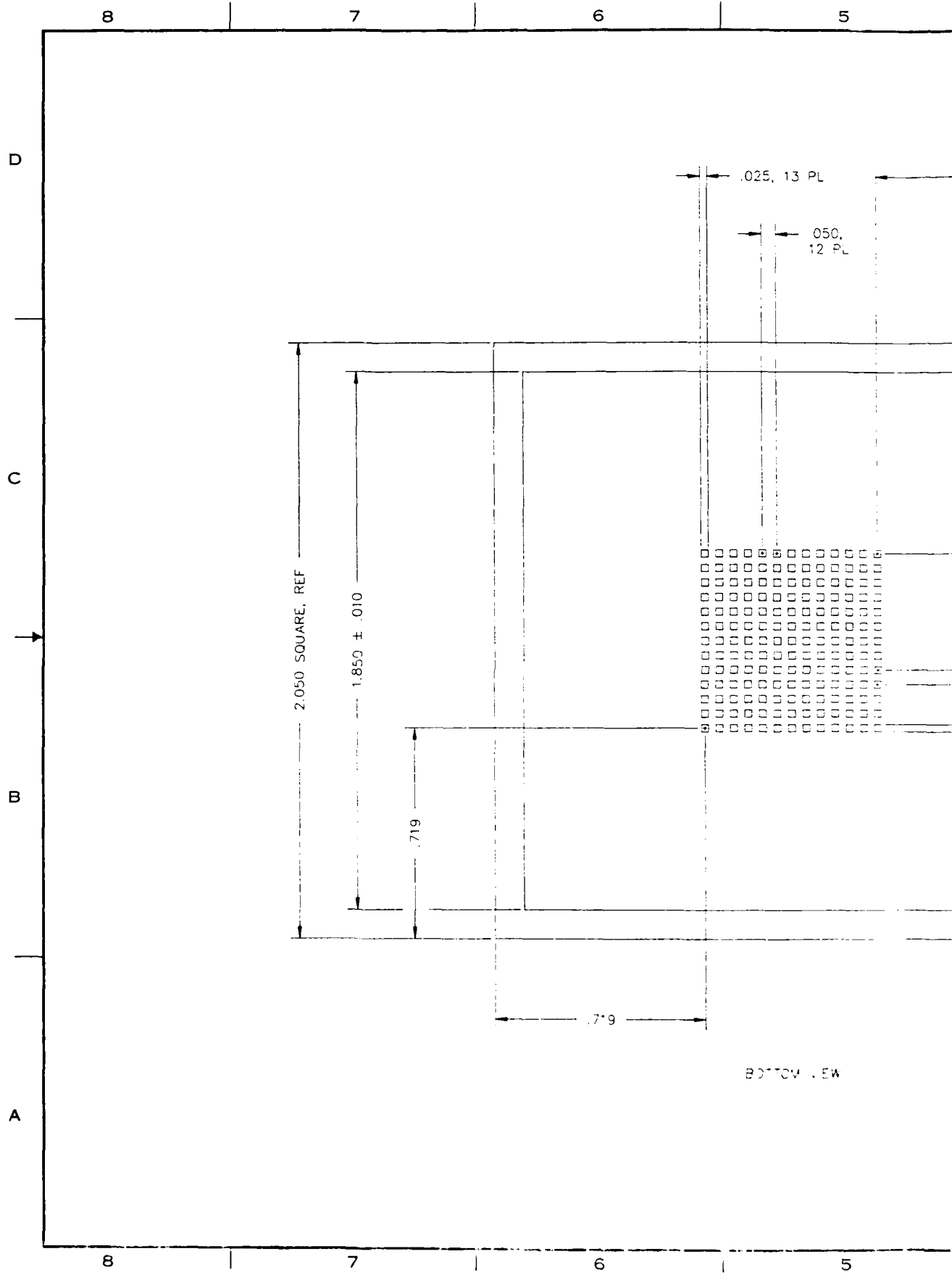




**B-6**

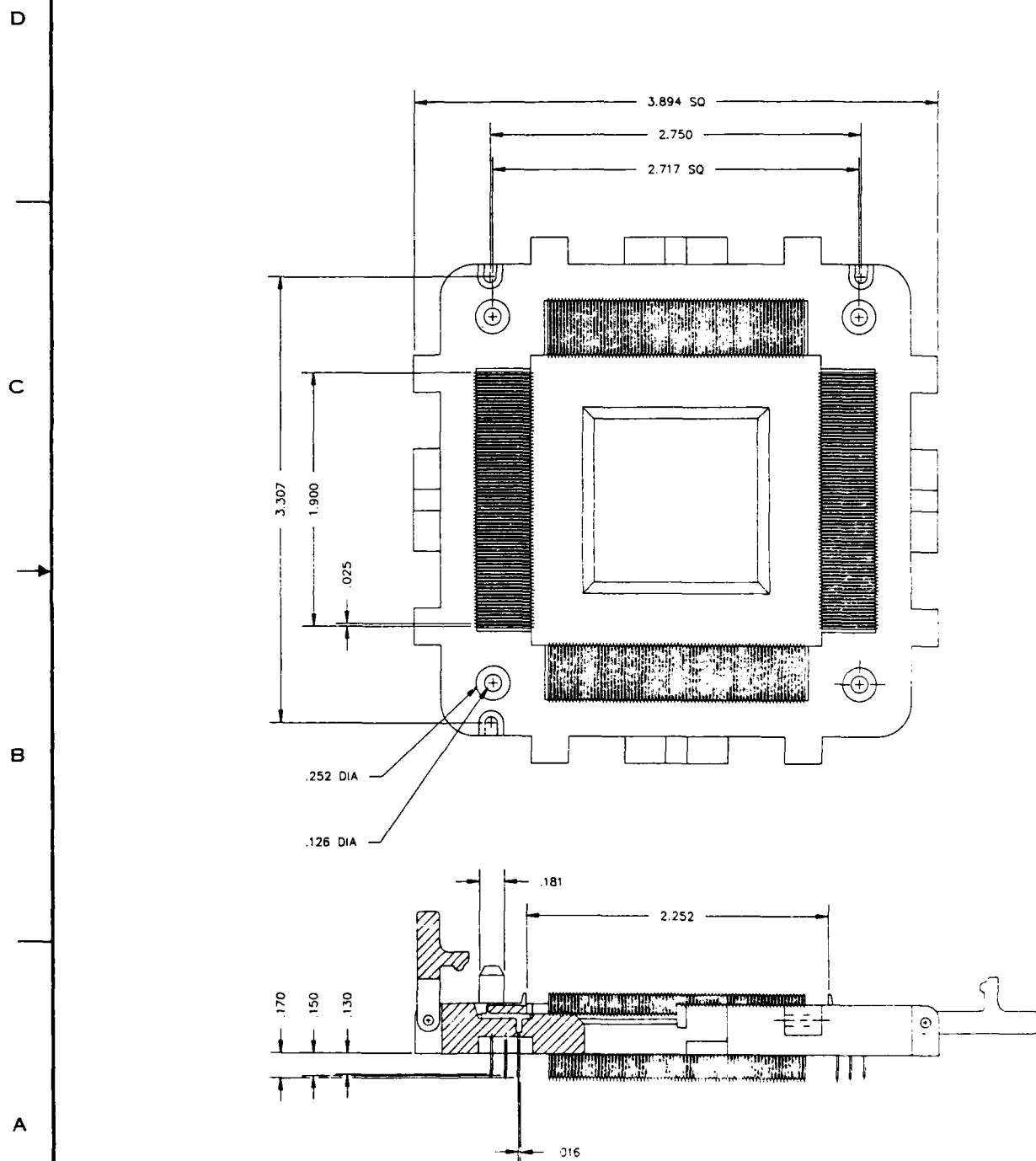
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<p>1. DIMENSIONS ARE IN INCHES</p> <p>2. DIMENSIONS IN PARENTHESES ARE FOR REFERENCE ONLY</p> <p>3. DIMENSIONS IN SQUARE BRACKETS ARE FOR REFERENCE ONLY</p> <p>4. DIMENSIONS IN CIRCLES ARE FOR REFERENCE ONLY</p> <p>5. DIMENSIONS IN TRIANGLES ARE FOR REFERENCE ONLY</p> <p>6. DIMENSIONS IN PARALLELOGRAMS ARE FOR REFERENCE ONLY</p> <p>7. DIMENSIONS IN OVALS ARE FOR REFERENCE ONLY</p> <p>8. DIMENSIONS IN HEXAGONS ARE FOR REFERENCE ONLY</p> <p>9. DIMENSIONS IN OCTAGONS ARE FOR REFERENCE ONLY</p> <p>10. DIMENSIONS IN STARS ARE FOR REFERENCE ONLY</p> <p>11. DIMENSIONS IN CIRCLES WITH A DIAGONAL LINE ARE FOR REFERENCE ONLY</p> <p>12. DIMENSIONS IN CIRCLES WITH A DIAGONAL LINE AND A DOT ARE FOR REFERENCE ONLY</p> <p>13. DIMENSIONS IN CIRCLES WITH A DIAGONAL LINE AND A CROSS ARE FOR REFERENCE ONLY</p> <p>14. DIMENSIONS IN CIRCLES WITH A DIAGONAL LINE AND A PLUS SIGN ARE FOR REFERENCE ONLY</p> <p>15. DIMENSIONS IN CIRCLES WITH A DIAGONAL LINE AND A MINUS SIGN ARE FOR REFERENCE ONLY</p> <p>16. DIMENSIONS IN CIRCLES WITH A DIAGONAL LINE AND A STAR ARE FOR REFERENCE ONLY</p> <p>17. DIMENSIONS IN CIRCLES WITH A DIAGONAL LINE AND A TRIANGLE ARE FOR REFERENCE ONLY</p> <p>18. DIMENSIONS IN CIRCLES WITH A DIAGONAL LINE AND A SQUARE ARE FOR REFERENCE ONLY</p> <p>19. DIMENSIONS IN CIRCLES WITH A DIAGONAL LINE AND A CIRCLE ARE FOR REFERENCE ONLY</p> <p>20. DIMENSIONS IN CIRCLES WITH A DIAGONAL LINE AND A CROSS WITH A DOT ARE FOR REFERENCE ONLY</p>				
<p>TEXAS INSTRUMENTS</p> <p>DAVIDSON, MO</p>		<p>DAVIDSON, MO</p> <p>D 96214 2795713</p>		

5 4 3 2 1

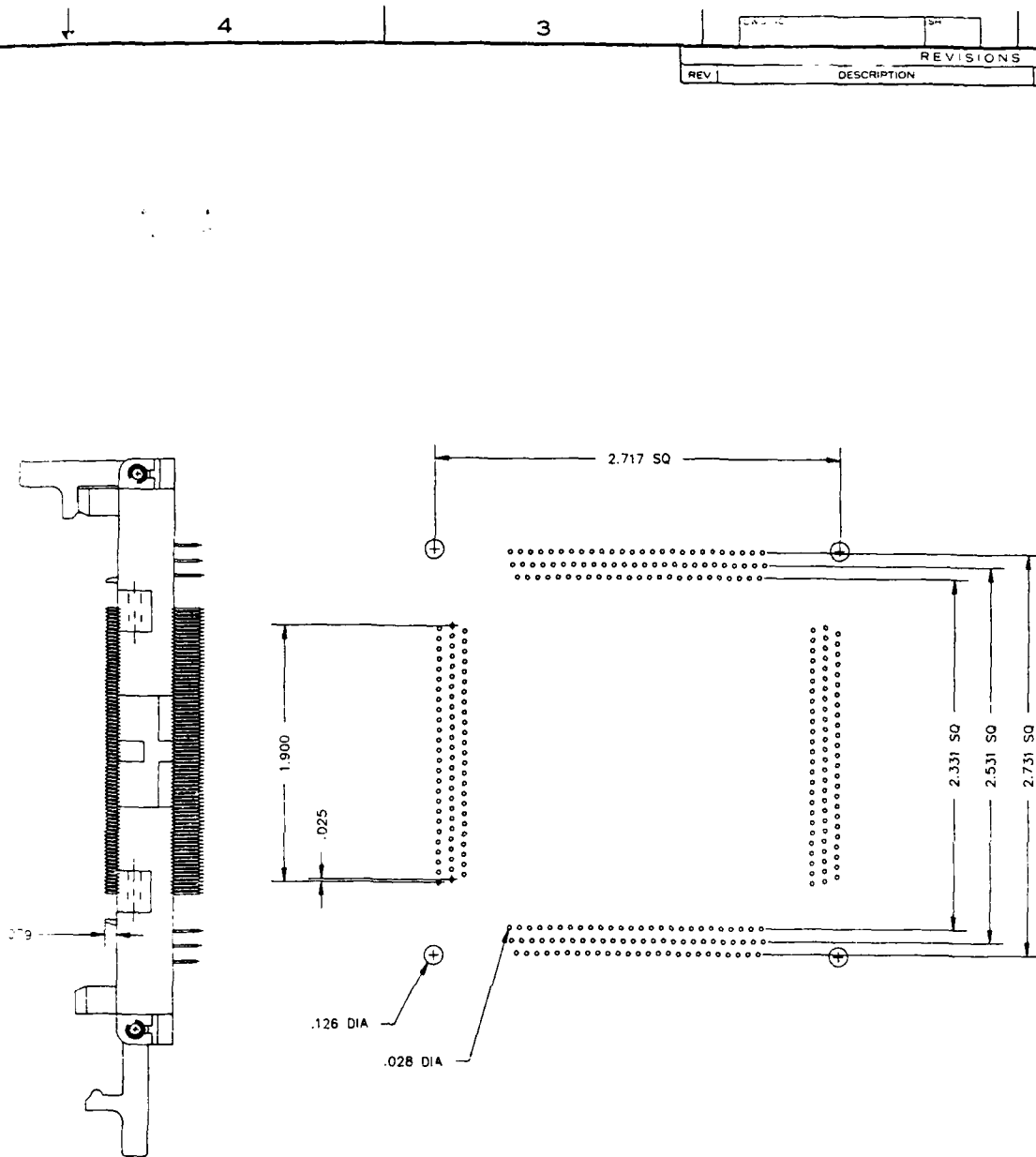




1. TOLERANCES TO BE  $\pm 0.3/\pm .012$



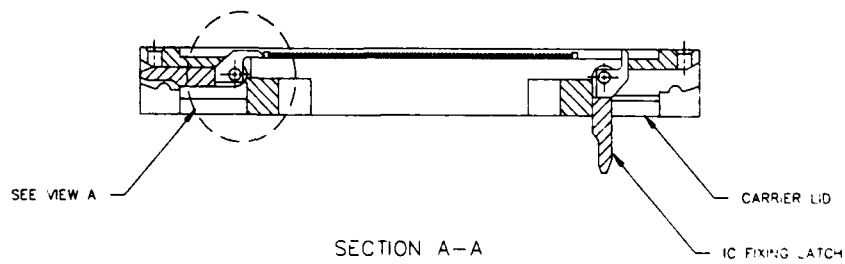
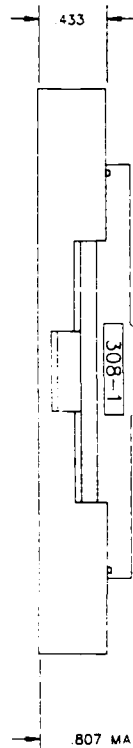
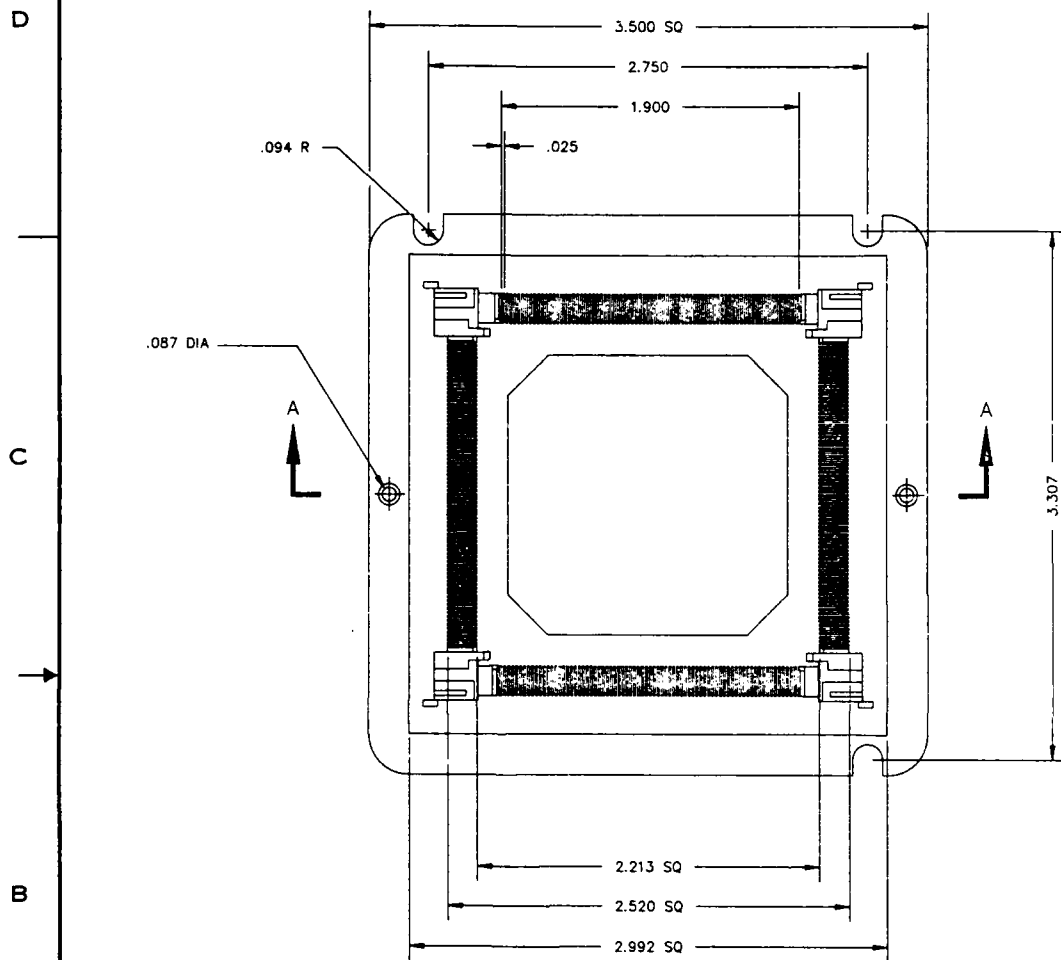
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					CLASSIFICATION				
					DESCRIPTION OF WORK				



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QTY						
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<p>UNLESS OTHERWISE SPECIFIED</p> <ul style="list-style-type: none"> <li>DIMENSIONS ARE IN INCHES</li> <li>TOLERANCES</li> <li>ANGLES 33°</li> <li>3 PLACE DECIMALS = .010</li> <li>2 PLACE DECIMALS = .02</li> <li>INTERPRET DRAWING PER DDG 1-1000</li> <li>REMOVE ALL BURRS AND SHARP EDGES</li> <li>WELDED JOINTS MAY BE DUE TO TENSILE STRESS</li> <li>IDENTICAL VIEWS APPLY WHERE PROVIDED</li> <li>IDENTICAL VIEWS TO BE IDENTICAL</li> </ul> <p>NOTE TO FRANCE</p> <p>004 006 008 010 012 014 016 018 020 022 024 026 028 030 032 034 036 038 040 042 044 046 048 050 052 054 056 058 060 062 064 066 068 070 072 074 076 078 080 082 084 086 088 090 092 094 096 098 100 102 104 106 108 110 112 114 116 118 120 122 124 126 128 130 132 134 136 138 140 142 144 146 148 150 152 154 156 158 160 162 164 166 168 170 172 174 176 178 180 182 184 186 188 190 192 194 196 198 200 202 204 206 208 210 212 214 216 218 220 222 224 226 228 230 232 234 236 238 240 242 244 246 248 250 252 254 256 258 260 262 264 266 268 270 272 274 276 278 280 282 284 286 288 290 292 294 296 298 300 302 304 306 308 310 312 314 316 318 320 322 324 326 328 330 332 334 336 338 340 342 344 346 348 350 352 354 356 358 360 362 364 366 368 370 372 374 376 378 380 382 384 386 388 390 392 394 396 398 400 402 404 406 408 410 412 414 416 418 420 422 424 426 428 430 432 434 436 438 440 442 444 446 448 450 452 454 456 458 460 462 464 466 468 470 472 474 476 478 480 482 484 486 488 490 492 494 496 498 500 502 504 506 508 510 512 514 516 518 520 522 524 526 528 530 532 534 536 538 540 542 544 546 548 550 552 554 556 558 560 562 564 566 568 570 572 574 576 578 580 582 584 586 588 590 592 594 596 598 600 602 604 606 608 610 612 614 616 618 620 622 624 626 628 630 632 634 636 638 640 642 644 646 648 650 652 654 656 658 660 662 664 666 668 670 672 674 676 678 680 682 684 686 688 690 692 694 696 698 700 702 704 706 708 710 712 714 716 718 720 722 724 726 728 730 732 734 736 738 740 742 744 746 748 750 752 754 756 758 760 762 764 766 768 770 772 774 776 778 780 782 784 786 788 790 792 794 796 798 800 802 804 806 808 810 812 814 816 818 820 822 824 826 828 830 832 834 836 838 840 842 844 846 848 850 852 854 856 858 860 862 864 866 868 870 872 874 876 878 880 882 884 886 888 890 892 894 896 898 900 902 904 906 908 910 912 914 916 918 920 922 924 926 928 930 932 934 936 938 940 942 944 946 948 950 952 954 956 958 960 962 964 966 968 970 972 974 976 978 980 982 984 986 988 990 992 994 996 998 1000</p>						

NOTES: UNLESS OTHERWISE SPECIFIED:

1. TOLERANCES TO BE  $\pm 0.3/\pm .012$



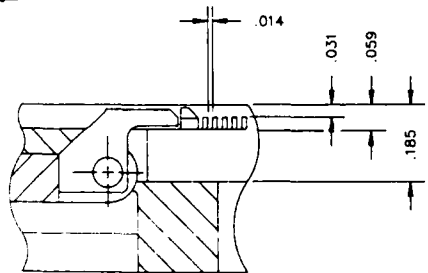
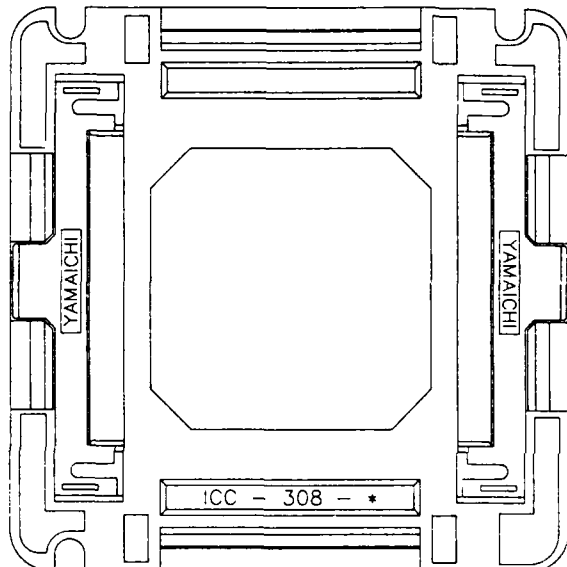
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VIEW A  
SCALE 5/1

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				PARTS LIST							
				UNLESS OTHERWISE SPECIFIED							
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				 TEXAS INSTRUMENTS (Dallas Texas)							
				CARRIER, LABCOM							
				303 LEAD							
				D 96214 2437706							






## 3. MATERIALS AND CONSTRUCTION:

Materials, finishes, and marking for each part shall be as specified herein. When the materials, or class of materials, are not specified, a material shall be used which will enable the device to meet all of the requirements of this drawing. Materials, finishes, and marking shall not blister, crack, flow, or be adversely affected when exposed to the storage, operating, or environmental conditions specified on this drawing.

## 4. KOVAR SEAL RING, MATERIALS AND CONSTRUCTION:


- 4.1 Seal ring shall be fabricated from Kovar and brazed to the top surface of the cofired alumina body of package as shown (Texas Instruments drawing 2795722 or 2795724).
- 4.2 Seal ring nominal outside dimension shall be as specified (TI drawing 2795722 or 2795724) and .042 maximum, .033 minimum in width. If an etching process is used in seal ring fabrication, undercutting of .005 maximum is allowable on each edge.
- 4.3 The outer radius on the corners of the seal ring must be no greater than .030 inch. The inner radius on the corners of the seal ring must be no less than .030 inch.
- 4.4 Entire assembly height ceiling is .115 inch maximum. Seal ring to be .040 inch thick nominally but may require grinding in some cases to limit assembly height to .115 inch.
- 4.5 Seal ring may be constructed of a single layer of Kovar or of two layers of Kovar brazed together as long as the minimum melting temperature of the braze is greater than 600 degrees C, and the overall thickness and thickness tolerance requirements are met.
- 4.6 Any brazing material used must have a melting temperature greater than 600 degrees C.
- 4.7 Nicks, dents or pits located on the outer half of the seal surface must conform to the following restrictions: (a) width does not exceed .008 inch, (b) length does not exceed .050 inch, (c) depth does not exceed .005 inch.
- 4.8 Vertical protrusions on the seal area greater than .002 inch are unacceptable.
- 4.9 The seal ring top surface must be flat within .004 inches per inch.
- 4.10 The seal ring must be plated on all exposed surfaces as per Section 7 of this document.

 <b>TEXAS INSTRUMENTS</b> <small>Dallas, Texas</small>	DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		<b>A</b>	<b>96214</b>	2795713	
			SCALE	NONE	SHEET	2

## 5. COFIRED ALUMINA PACKAGE BODY, MATERIALS AND CONSTRUCTION:

- 5.1 The cofired alumina body of the chip carrier shall consist of seven (7) ceramic layers and seven (7) metallization patterns.
- 5.2 The ceramic layers shall be .007 inch thick nominal with a thickness tolerance of  $\pm 10\%$ .
- 5.3 The alumina shall preferably be white 92% minimum alumina but a different grade or color of alumina may be used provided the dielectric constant is a maximum of 9.5 at 1MHz.
- 5.4 The thick film metallization refractory material used shall have a maximum resistivity of 15 milliohms per square as fired.
- 5.5 The outside dimension of all layers of the cofired body shall be as specified (TI drawing 2795722 or 2795724) with a tolerance of  $\pm 0.8\%$ .
- 5.6 Three of the four corners of the cofired body shall be square with the fourth corner serving as an index corner and being chamfered at .020 inch x 45 degrees.
- 5.7 The ceramic layers shall be identified as numbers 1 through 7 with layer number 1 being the bottom layer onto which the thermal base is brazed and layer 7 being the top layer onto which the Kovar seal ring and leads are brazed.
- 5.8 The nominal cavity sizes of the seven ceramic layers are as follows:
- 5.8.1 196 lead package (TI drawing 2795724):

- Layer 1 - 1.100 nominal  $\pm .009$  with .102 x 45 degrees nominal chamfer on all corners
- Layer 2 - 1.100 nominal  $\pm .009$  with .102 x 45 degrees nominal chamfer on all corners
- Layer 3 - 1.100 nominal  $\pm .009$  with .102 x 45 degrees nominal chamfer on all corners
- Layer 4 - 1.100 nominal  $\pm .009$  with .102 x 45 degrees nominal chamfer on all corners and a .065 x .075 cutout at 45 degrees on each corner with the .065 dimension centered along the .144 long hypotenuse of the chamfer
- Layer 5 - 1.100 nominal  $\pm .009$  with .102 x 45 degrees nominal chamfer on all corners and a .065 x .075 cutout at 45 degrees on each corner with the .065 dimension centered along the .144 long hypotenuse of the chamfer


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- Layer 6 - 1.150 nominal +/- .010 with chamfer on all four corners of a size to expose the entire capacitor cavity (cutout) of layers 3, 4 and 5 (approximately .050 x 45 degrees)
- Layer 7 - 1.150 nominal +/- .010 with chamfer on all four corners of the same size as in layer 6

5.8.2 308 lead package (TI drawing 2795722):


- Layer 1 - 1.650 nominal +/- .013 with .102 x 45 degrees nominal chamfer on all corners
- Layer 2 - 1.650 nominal +/- .013 with .102 x 45 degrees nominal chamfer on all corners
- Layer 3 - 1.650 nominal +/- .013 with .102 x 45 degrees nominal chamfer on all corners and a .065 x .075 cutout at 45 degrees on each corner with the .065 dimension centered along the .144 long hypotenuse of the chamfer
- Layer 4 - 1.650 nominal +/- .013 with .102 x 45 degrees nominal chamfer on all corners and a .065 x .075 cutout at 45 degrees on each corner with the .065 dimension centered along the .144 long hypotenuse of the chamfer
- Layer 5 - 1.650 nominal +/- .013 with .102 x 45 degrees nominal chamfer on all corners and a .065 x .075 cutout at 45 degrees on each corner with the .065 dimension centered along the .144 long hypotenuse of the chamfer
- Layer 6 - 1.710 nominal +/- .014 with chamfer on all four corners of a size to expose the entire capacitor cavity (cutout) of layers 3, 4 and 5 (approximately .050 x 45 degrees)
- Layer 7 - 1.710 nominal +/- .014 with chamfer on all four corners of the same size as in layer 6

- 5.9 A radius of .010 inch is allowed on the corners of the capacitor cutouts occurring in layers 3, 4 and 5 of both packages.
- 5.10 The metallization patterns shall be identified as follows: MP-IX being the metallization on the bottom side of ceramic layer 1 (braze ring for thermal base) and as MP-1 through MP-7 being the metallization on top of ceramic layers 1 through 7.
- 5.11 The dielectric pattern on the bottom side of the base of the package shall be referred to as pattern CP-B and shall serve as a mask to expose the metallized package mounting pads.
- 5.12 The features contained in the 8 metallization patterns are as follows:  
 MP-IX - Metallization ring for brazing on of thermal base


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- MP-1 - Tertiary power ring
- MP-2 - Secondary power ring, capacitor pads
- MP-3 - Primary power ring
- MP-4 - Lower ground ring
- MP-5 - Bonding shelf, signal and power and ground conductor lines for connection to drop in circuit
- MP-6 - Upper ground ring
- MP-7 - I/O pads for brazing on of lead frames, Metallization for brazing on of Kovar seal ring


- 5.13 Metallization patterns and via locations to be as specified (TI drawing 2795722 or 2795724).
- 5.14 The widths of the signal, power and ground conductor lines on metal layer MP-5 are to be as specified (TI drawing 2795722 or 2795724).
- 5.15 The metallization on layer MP-5 shall have a nominal pullback of .005 inch from the cavity edge, not less than .0005 inch.
- 5.16 All designated internal vias shall have a maximum resistance of 8 milliohms per via.
- 5.17 No castellations or side metallization are required for this package. Side metallization is acceptable.
- 5.18 All exposed metallization on the ceramic body shall be plated as per section 7 of this document.
- 5.19 Total length and width camber of ceramic shall be no greater than .004 inches per inch.
- 5.20 Electrical leakage between any adjacent conductors and conductors to seal ring shall not exceed 5 nano-amps at 100 Volts DC.
- 5.21 There shall be no burrs greater than .005 inch on outside corner chamfers or edges.
- 5.22 There shall be no delamination or cracking of the assembly prior to or following exposure to processing temperatures and service environments.
- 5.23 Edge cracks due to cutting or scoring shall not exceed .015 inch.
- 5.24 Peripheral chips shall not exceed .050 length x .015 depth x .015 width. Corner chips shall not exceed .030 x .030 x .020.
- 5.25 A minimum of 70% of the width of the first .015 inch length of a conductor line, from the cavity out, shall be void free when viewed at 10x.

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- 5.26 There shall be no protrusions greater than .001 inch in height on the first .015 inch length of a lead trace, from the cavity out.
- 5.27 Conductor lines shall not contain voids, pin holes, nodules or scratches which reduce the effective width of any conductor by more than 50%. Enlarged conductor lines used for power and ground should not be reduced by more than 20%.
- 5.28 There shall be no flaking, peeling or blistering on the gold when viewed at 10x magnification, and no discoloration visible to the unaided eye.
- 5.29 The package shall present a clean appearance and shall contain no loose foreign material and contamination that cannot be removed by ultrasonic cleaning.
6. LEAD FRAME, MATERIALS AND CONSTRUCTION:
- 6.1 The lead frame is to be fabricated from Kovar and brazed to the top surface of the cofired ceramic body of the package as shown (TI drawing 2795722 or 2795724).
- 6.2 The lead frames must be plated on all exposed surfaces as per section 7 of this document.
- 6.3 The lead frame material shall be .005 inch thick nominal. If lead is etched, undercutting of .001 inch maximum on each edge is allowable
- 6.4 The leads are to be on .025 inch centers with configuration as shown (TI drawing 2795722 or 2795724).
- 6.5 The leads shall be .010 inch nominal in width with .015 inch nominal space.
- 6.6 The entire lead frame shall preferably be of a single piece of material incorporating all four sides. This will ensure exact orientation of all of the leads with respect to each other. Four individual lead frames may also be used but the maximum tolerance from one lead location to any other lead location may not be greater than +/- .001 inch.
- 6.7 The leads must be a nominal of .300 inch long with a .150 inch width minimum tie bar along the outside edge as shown (TI drawing 2795722 or 2795724).
- 6.8 Registration holes in the tie bar area are acceptable.
- 6.9 Leads must exhibit a perpendicular pull strength of 0.5 lb-force minimum.

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- 6.10 Leads shall be flat and exhibit no kinks or permanent deformation. Protrusions greater than .002 inch on any surface of a lead are unacceptable.
7. THERMAL BASE, MATERIALS AND CONSTRUCTION:
- 7.1 The thermal base may be made of either Beryllia or 90/10 Tungsten Copper (Elkonite).
- 7.2 If Beryllia is used, the top surface must be fully metallized and connected to package ground. The bottom surface must be metallized and masked to expose a prescribed thermal pad pattern (TI drawing 2795722 or 2795724). The bottom surface must also be connected to package ground either through the use of continuous metallization around the edges of the base or by through vias in the brazing area. Vias shall not exist in exposed area of the main package cavity.
- 7.3 If Tungsten/Copper is used, it must be treated as required to ensure hermeticity and it must also be connected to package ground. The bottom side must be masked to expose a prescribed thermal pad pattern (TI drawing 2795722 or 2795724).
- 7.4 Other thermally conductive materials which exhibit a closely matched coefficient of thermal expansion to the ceramic body of the chip carrier may be proposed for use by the supplier. The material will be reviewed by TI and may be used only with subsequent written approval from TI.
- 7.5 All exposed metal or metallization on the thermal base must be plated as per section 7 of this document.
- 7.6 If beryllia is used, the base shall be .020 thick nominal with a maximum tolerance of  $\pm .002$  inch. If Tungsten/Copper is used it may be either .015 or .020 inch thick nominal with a maximum tolerance of  $\pm .002$  inch.
- 7.7 The base shall be designed such that the corner of the base does not extend beyond the cofired ceramic body at the index corner chamfer.
- 7.8 The base shall have a maximum camber of .004 inches per inch.
8. PLATING:
- 8.1 All exposed metal on finished package including lead frames, seal ring, refractory metal and thermal base must be plated first with electroless or electrolytic Nickel as specified in QQ-N-290, with a minimum thickness of 50 microinches to a maximum of 350 microinches. Gold shall be plated over the

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Nickel in accordance with MIL-G-45204, Type III, Grade A at a thickness of 50 microinches minimum.

9. ENVIRONMENTAL REQUIREMENTS:

9.1 Hermeticity: Maximum helium leakage rate shall not exceed  $1 \times 10^{-8}$  cc/second helium. The test shall be per MIL-STD-883, Method 1014, condition A4.

9.2 Constant Acceleration: The package shall not exhibit any cracking, delamination or changes in electrical characteristics when subjected to constant acceleration per MIL-STD-883, Method 2001, Condition E.

9.3 Thermal Shock: The package shall not exhibit any cracking, delamination, or changes in electrical characteristics when subjected to sudden changes in temperature per MIL-STD-883, Method 1011, Condition C.

9.4 Temperature Cycling: The package shall not exhibit any cracking, delamination, or changes in electrical characteristics when subjected to extreme temperature variations per MIL-STD-883, Method 1010, Condition C.

9.5 Salt Atmosphere: The package shall not exhibit any evidence of corrosion contributing to electrical failure, following exposure to 24 hours of salt atmosphere per MIL-STD-883, Method 1009, Condition A.


9.6 Solderability: The package must conform to solderability requirements of MIL-STD-883, Method 2003 with the exception of the aging test (paragraph 3.2).

10. COMPLIANCE:

10.1 The supplier shall comply with all construction and workmanship requirements outlined in this specification.

10.2 All material used in the construction of the chip carriers shall be unused and undamaged, shall be of a quality consistent with proposed use and performance specified, and shall comply completely with applicable specifications. Materials and processes shall be subject at any time to such tests of the pertinent specification as may be prescribed by Texas Instruments to determine compliance with specification requirements. Also, if the supplier discovers faulty or nonconforming materials or processes, he shall report the same to Texas Instruments, if the defective product was previously shipped.

10.3 Supplier is to notify Texas Instruments before making any change in plating processes or plating type.

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11. PREPARATION FOR DELIVERY:

11.1 Packaging: Packaging shall be adequate to provide protection against any damage, breakage, or loss during shipment from the supply source to the ultimate using activity.


11.2 Marking: Each shipping container shall be legibly marked in accordance with MIL-STD-130 with the following information:

TI part number

Manufacturers identification and date code (lot number)

12. NOTES:

12.1 All chamfers are dimensioned as 'length of sides x cutting angle', where the length of sides is in the x or y direction and is not the hypotenuse of the chamfer triangle.

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SUGGESTED SOURCES OF SUPPLY:

1. Interamics (201726)  
11391 Sorrento Valley Road  
San Diego, CA 92121
2. Ceramic Systems (No FSCM No.)  
2780 Coronado Road  
Anaheim, CA 92806

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## 3. REQUIREMENTS:

## 3.1 MATERIALS AND CONSTRUCTION:

Materials, finishes, and marking for each part shall be as specified herein. When the materials, or class of materials, are not specified, a material shall be used which will enable the device to meet all of the requirements of this drawing. Materials, finishes, and marking shall not blister, crack, flow, or be adversely affected when exposed to the storage, operating, or environmental conditions specified on this drawing.

## 3.1.1 PHYSICAL CONFIGURATION: To fit package, per Figures 1 and 2.

3.1.1.1 Assembly shall consist of socket base and either one carrier lid which will accommodate the package with formed or unformed leads, or a pair of carriers, one which will accommodate a package with formed leads and one which will accommodate a package with unformed leads

## 3.1.2 MATERIALS:

3.1.2.1 BODY: Polyethersulfone G. F.

3.1.2.2 CONTACTS: Beryllium copper per QQ-C-533

3.1.2.3 LID AND LID LOCATION POST WITH SCREW: Nickel plated brass

## 3.1.3 FINISHES:

3.1.3.1 CONTACTS: 50 microinches minimum gold plating per MIL-G-45204 over 50 microinches minimum/350 microinches maximum nickel plating per QQ-N-290

## 3.2 MARKING:

ALL PACKAGES SHALL BE MARKED IN ACCORDANCE WITH MIL-STD-130 WITH THE FOLLOWING INFORMATION:

3.2.1 MANUFACTURER'S PART NUMBER


3.2.2 MANUFACTURER'S NAME

## 3.3 ELECTRICAL:

3.3.1 CONTACT RESISTANCE: Not greater than 30 milliohms

3.3.2 CAPACITANCE: 0.5 picofarads

3.3.3 INSULATION RESISTANCE: 1000 megohms minimum at 500 volts DC

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3.3.4 BREAKDOWN VOLTAGE: 1000 volts

3.3.5 OPERATING TEMPERATURE: -55 to +125 degrees C

4. QUALITY ASSURANCE PROVISIONS:

4.1 RESPONSIBILITY FOR INSPECTION:


Unless otherwise specified in the contract or purchase order, the supplier is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified in the contract or order, the supplier may use his own or any other facilities suitable for the performance of the inspection requirements specified herein, unless disapproved by the procuring activity. The procuring activity reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

5. PREPARATION FOR DELIVERY:

5.1 Packaging shall be adequate to provide protection against any damage, breakage, or loss during shipment from the supply source to the ultimate using activity.

6. NOTES:

6.1 Identification of the suggested source(s) of supply hereon is not to be construed as a guarantee of present or continued availability as a source of supply for the item(s).

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NOTES:

1. THIS PACKAGE SHALL BE FABRICATED IN ACCORDANCE WITH TI SPECIFICATION 2795713.
2. AREA WITHIN CIRCLE SHOWS LEAD AFTER FORMING AND CLIPPING.

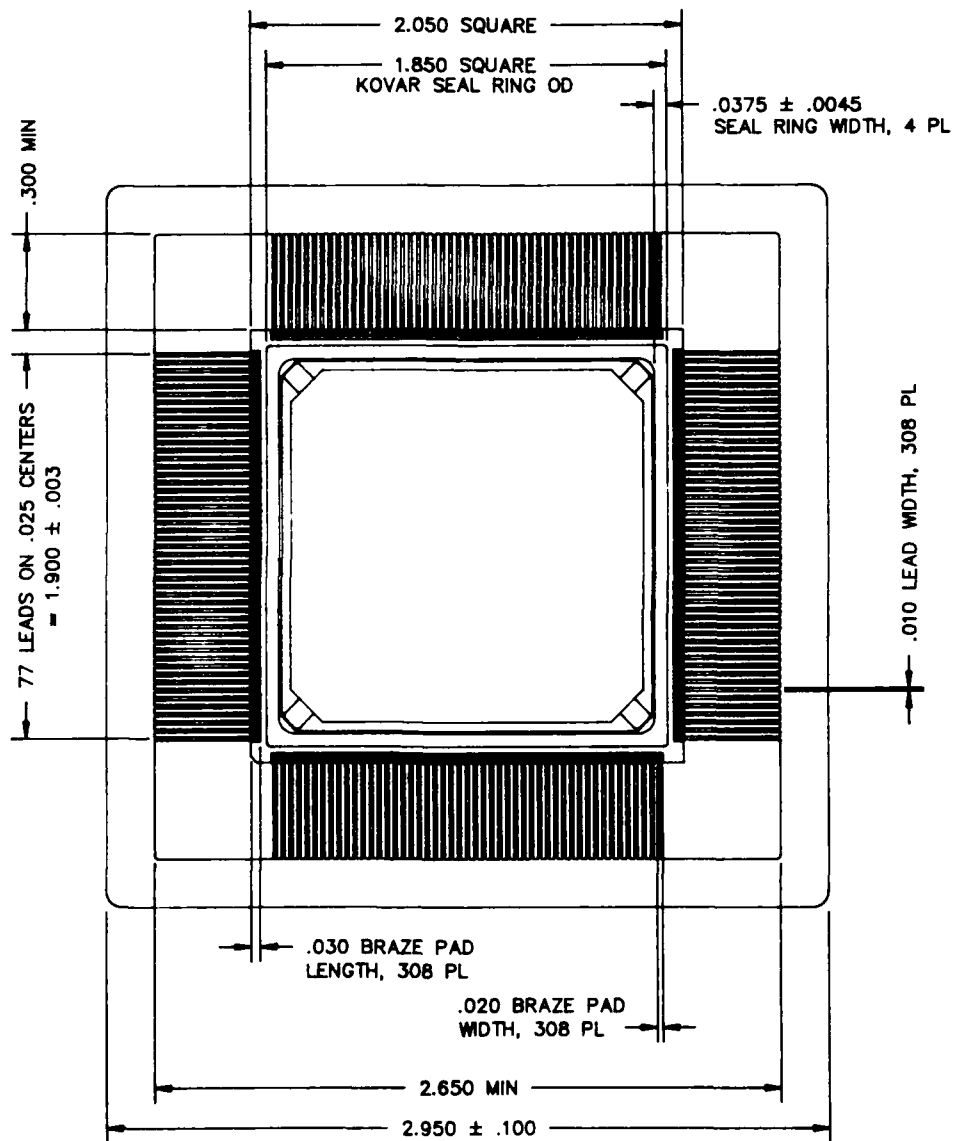


FIGURE 1

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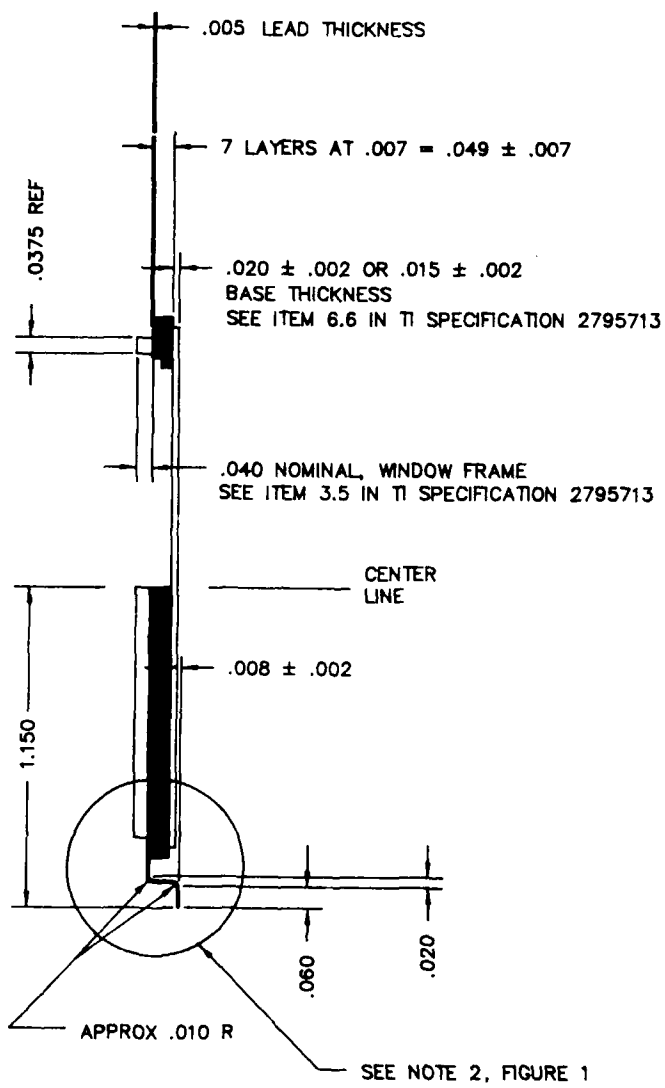




FIGURE 2

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			SCALE	NONE	SHEET	5.

SUGGESTED SOURCE(S) OF SUPPLY:

1. NEPENTHE (No FSCM No.)  
2471 East Bayshore Road, Suite 520  
Palo Alto, California 94303

PART NO.	MANUFACTURER'S PART NO.	
	SOURCE 1	SOURCE 2

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APPLICATION		REVISIONS			
NEXT ASSY	USED ON	REV	DESCRIPTION	DATE	APPROVED
	1009				

1. SCOPE

This specification covers the requirements for a stepped lid.

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of the specification to the extent specified herein. In the event of any conflict between this document and the reference documents, this document shall govern.

MIL-STD-883	TEST METHODS AND PROCEDURES FOR MICROELECTRONICS
MIL-STD-129	MARKING FOR SHIPPING AND STORAGE
MIL-G-45204	GOLD PLATING, ELECTRODEPOSITED
QQ-N-290	NICKEL PLATING, ELECTRODEPOSITED
ASTM-F15-61T	STANDARD SPECIFICATION FOR KOVAR

SOURCE CONTROL DRAWING

REV																			
SHEET																			
REV STATUS OF SHEETS	REV																		
	SHEET	1	2	3	4	5	6	7	8	9									
UNLESS OTHERWISE SPECIFIED • DIMENSIONS ARE IN INCHES • TOLERANCES ANGLES ±1° 3 PLACE DECIMALS ± 010 2 PLACE DECIMALS ± 02 • PARENTHEICAL INFO FOR REF ONLY	DWN	DATE																	
	CHK																		
	ENGR																		
	APVD																		
	QA	CM																	
	CONTR																		
RLSE																			
<div style="text-align: center;"> <b>TEXAS INSTRUMENTS</b>  <i>Dallas, Texas</i> </div> <div style="text-align: center; margin-top: 10px;">           HEADER, LID, STEPPED         </div>		SIZE	FSCM NO	DRAWING NO															
		<b>A</b>	<b>96214</b>	2891091															
		SCALE	SHEET 1 of 9																



## 3. REQUIREMENTS

## 3.1 MATERIALS AND CONSTRUCTION:

Materials, finishes and marking for each part shall be as specified herein. When the materials or classes of materials are not specified, a material shall be used which will enable the device to meet all of the requirements of this drawing. Materials, finishes and marking shall not blister, crack, flow or be adversely affected when exposed to the storage, operating or environmental conditions specified in this drawing.

3.1.1 Physical Configuration:  
See Figure 1 and Table II.

## 3.1.2 Materials and Finishes:

3.1.2.1 Lid:  
Kovar Type per ASTM-F15-61T.3.1.2.2 Plating:  
Lid shall be plated per Table II in one of the following configurations:

Configuration 1: Electrolytic Nickel per QQ-N-290 Class 2, 100 microinches minimum, 350 microinches maximum

Configuration 2: Electroless Nickel per QQ-N-290 Class 1, 100 microinches minimum, 350 microinches maximum

Configuration 3: Gold per MIL-G-45204 Type 1 Class 1, 50 microinches minimum over Electrolytic Nickel per QQ-N-290 Class 2, 100 microinches minimum, 350 microinches maximum

Configuration 3: Gold per MIL-G-45204 Type 1 Class 1, 50 microinches minimum over Electroless Nickel per QQ-N-290 Class 1, 100 microinches minimum, 350 microinches maximum

## 3.2 ELECTRICAL:

## 3.2.1 No requirements.

## 3.3 MECHANICAL:

## 3.3.1 Lids shall be capable of meeting all tests listed in Table I of this specification.

## 3.3.2 Flatness to be per Figure 1.

## 3.4 VISUAL INSPECTION:

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### 3.4.1 Lid Surface Conditions:

#### 3.4.1.1 Damage (Inspection at IX):

3.4.1.1.1 Nicks, dents or pits located on the outer 1/2 of the seal surface must conform to the following restrictions: (a) width does not exceed .008, (b) length does not exceed .050, (c) depth does not exceed .005.

3.4.1.1.2 Nicks, dents or pits located on the inner 1/2 of the seal surface have only the restrictions listed in paragraph 3.4.1.1.4.

3.4.1.1.3 Nicks, dents or pits located on the lid, other than the seal area, cannot exceed .010 in diameter.

3.4.1.1.4 All protrusions greater than .004 are unacceptable.

3.4.1.1.5 Any foreign particles are unacceptable.

#### 3.4.1.2 Stains:

3.4.1.2.1 Stains (discolorations on the lid which cannot be removed using common cleaning practices) are unacceptable.

3.4.1.2.2 Fingerprints are not stains.

3.4.1.2.3 Variations in the grain structure, or the gold color of the plating are not stains.

#### 3.4.1.3 Plating:

3.4.1.3.1 There shall be no flaking, pitting, lifting or peeling of the plating.

3.4.1.3.2 There shall be no plating blisters or bubbles that may be peeled off of the base metal.

3.4.1.3.3 There shall be no non-conductive inclusions in the plating.


3.4.1.3.4 There shall be no exposed underplate or base material greater than .007 in diameter.

3.4.1.3.5 There shall be no plating discoloration in the seal areas.

3.4.1.3.6 There shall be no corrosion.

### 3.5 SCREENING:

#### 3.5.1 Visual Inspection:

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3.5.1.1 The parts shall be 100% inspected by the vendor for compliance with paragraphs 3.4.1.1.1, 3.4.1.1.2, 3.4.1.1.3 and 3.4.1.1.4 of this specification.

3.5.1.2 The parts shall be inspected by the vendor on a sample basis for compliance with all paragraphs of section 3.4 with the exception of those listed in paragraph 3.5.1.1. Parts from each plating lot shall be inspected on a sample basis of 3(0) acceptance.

3.6 LOT ACCEPTANCE:

3.6.1.1 Lot Acceptance per paragraph 4.3 herein.

3.7 QUALIFICATION:

3.7.1 When specified on the purchase order the lot will be subjected to additional testing per paragraph 4.3.2. This testing is only required for the initial qualification.

3.8 DOCUMENTATION:

3.8.1 Certificate of Conformance:

3.8.1.1 Certificate of Conformance per paragraph 4.4.2 herein.

3.8.2 Traceability:

3.8.2.1 Traceability per paragraph 4.4.1 herein.


4. QUALITY ASSURANCE PROVISIONS

4.1 RESPONSIBILITY FOR INSPECTION:

4.1.1 Unless otherwise specified in the purchase order, the supplier is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified in the contract or order, the supplier may use his own or any other facilities suitable for the performance of the inspection requirements specified herein, unless disapproved by the procuring activity. The procuring activity reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

4.2 CHANGE NOTICE:

4.2.1 The manufacturer shall notify the procuring activity prior to the delivery of the parts of any changes in the design, material or process that may affect performance, quality or reliability of the part specified herein. Proprietary information need not be disclosed, however, the procuring activity requires that sufficient

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information be made available to determine the effect on any equipment which utilizes this part.

#### 4.3 QUALITY CONFORMANCE INSPECTION:

##### 4.3.1 Lot Acceptance:

4.3.1.1 A sample from each plating lot shall be evaluated per Table I.

4.3.1.2 As a minimum, each plating lot will have passed subgroups 1, 2, 3 and 4 of Table I.

##### 4.3.2 Qualification:

4.3.2.1 Qualification testing will consist of all tests specified before with the addition of Subgroups 5 and 6 of Table I. This testing is only required for the initial qualification. A change in material or plating would require requalification.

#### 4.4 TRACEABILITY / DATA SUBMISSION:

##### 4.4.1 Traceability:

4.4.1.1 Each lid shall be traceable to a manufacturer's plating lot.

##### 4.4.2 Certificate of Conformance:

4.4.2.1 A certificate of compliance shall accompany each lot/shipment. This document will be signed by a QRA representative who is attesting to the performance and passing of the screening and lot acceptance requirements herein.

#### 5. PREPARATION FOR DELIVERY


##### 5.1 PACKAGING:

5.1.1 Packaging shall be adequate to provide protection against any damage, breakage or loss during shipment from the supply source to the ultimate using activity.

##### 5.2 MARKING:

5.2.1 Each individual container shall be marked in accordance with MIL-STD-129 displaying the following information:

Texas Instruments part number  
Vendor identification  
Plating lot identification (eg. date code)  
Lot identification number

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## 5.3 DOCUMENTATION:

5.3.1 A Certificate of Conformance will be shipped with each lot.

## 6. NOTES


6.1 Only the item described on this drawing, when procured from the vendor(s) listed herein, is approved by TEXAS INSTRUMENTS INCORPORATED for use in the application(s) specified herein. A substitute item shall not be used without prior approval by TEXAS INSTRUMENTS INCORPORATED.

6.2 Identification of the APPROVED SOURCE(S) OF SUPPLY herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item described on the drawing.

6.3 This lid is for use in hybrid and microelectronics manufacturing.

TABLE 1  
LOT ACCEPTANCE TESTS  
MIL-STD-883

SUBGROUP	TEST	METHOD	CONDITION	QTY(#ACC)
1	Physical Dimensions	2016		15(0)
2	Solderability	2003	245 +/- 5 degrees C	3(0)
3	Thermal Shock	1011	C	3(0)
	Bake	1008	150 degrees C 2 hours	
	Seal	1014	A4	
4	Moisture Resistance	1004		3(0)
5	Salt Atmosphere	1009		5(0)

 <b>TEXAS INSTRUMENTS</b> <small>Dallas, Texas</small>	OWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		A	96214	2891091	
			SCALE	SHEET		6 of 9

DWG NO

2891091

SH 7

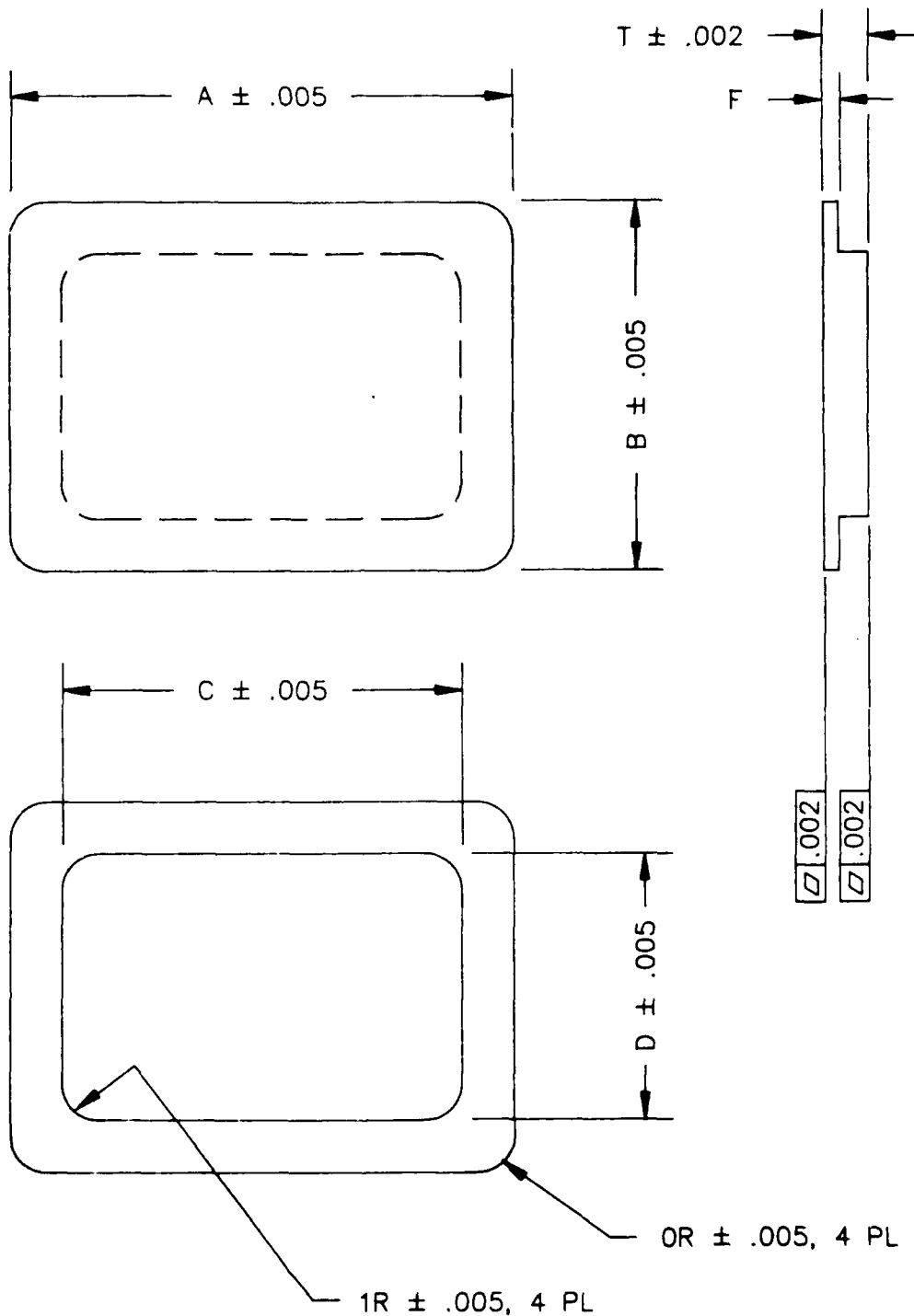


FIGURE 1

<b>TEXAS INSTRUMENTS</b> Dallas, Texas	DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		<b>A</b>	<b>96214</b>	2891091	
SCALE			SHEET		7 of 9	

T-28483

B-32

TABLE II

DASH NUMBER	A	B	C	D	OR	IR	Fmin	Fmax	T
-01	.885	.845	.785	.745	.017	.035	.0035	.0055	.010
-02	.885	.845	.785	.745	.017	.035	.0035	.0055	.015
-03	.870	.870	.785	.785	.017	.035	.0035	.0055	.010
-04	.900	.900	.790	.790	.010	.050	.005	.005	.010
-05	.885	.845	.785	.745	.017	.050	.0035	.0055	.010
-06	.900	.900	.790	.790	.010	.050	.005	.005	.010
-07	1.245	1.245	1.145	1.145	.018	.044	.0035	.0055	.015
-08	1.845	1.845	1.745	1.745	.018	.044	.0035	.0055	.015
-09	1.395	.645	1.220	.470	.018	.044	.0035	.0055	.015
-10	.865	.835	.750	.720	.018	.044	.0035	.0055	.015
-11	2.135	1.135	2.035	1.035	.018	.044	.0035	.0055	.015
-12	2.135	1.135	2.035	1.035	.018	.044	.0035	.0055	.015
-13	1.240	1.240	1.145	1.145	.018	.044	.0035	.0055	.015
-14	1.840	1.840	1.745	1.745	.018	.044	.0035	.0055	.015



DWN DATE

ISSUE DATE

SIZE

A

FSCM NO

96214

DRAWING NO

2891091

REV


SCALE

SHEET 8 of 9

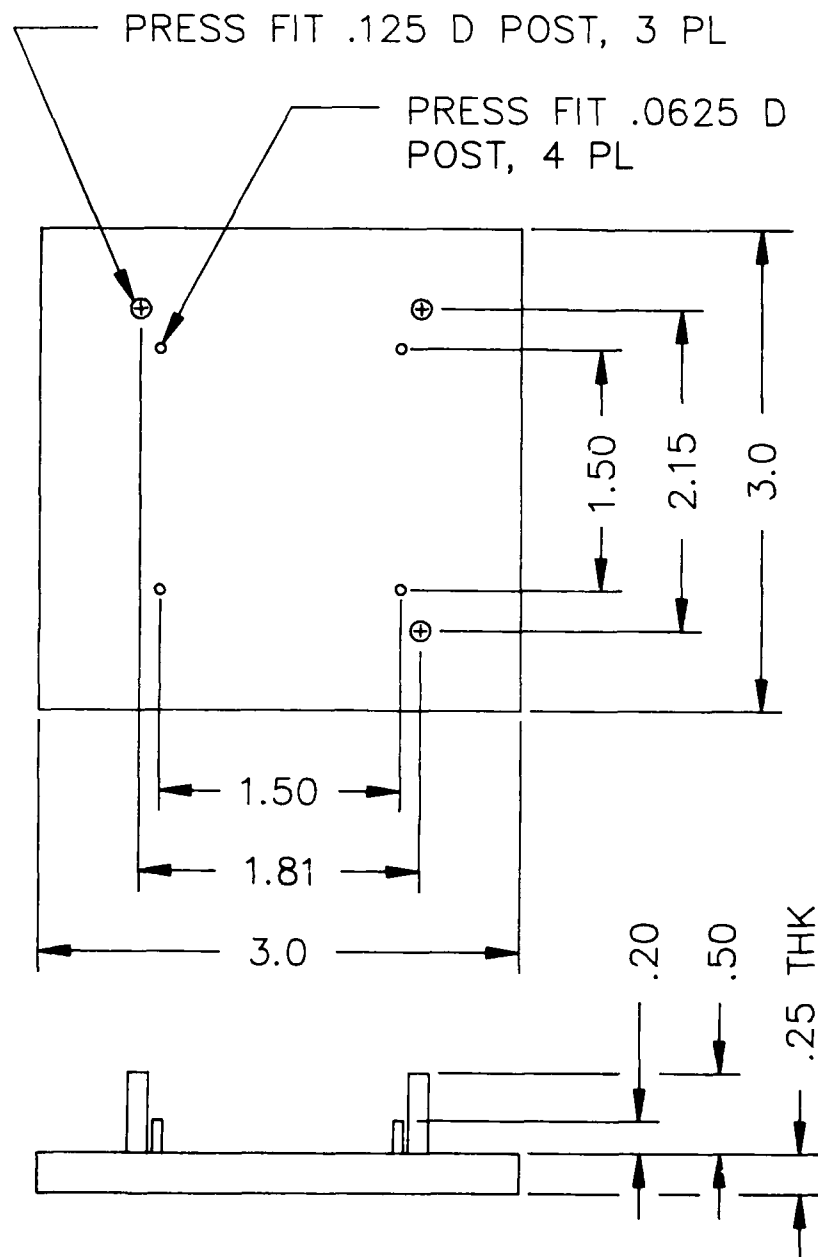
## APPROVED SOURCE(S) OF SUPPLY:

1. Isotronics Incorporated (017331)  
Industrial Park  
New Bedford, MA 02745
2. Hi-Rel Products Incorporated (062590)  
16 Plains Road  
Essex, CT 06426

PART NUMBER	MANUFACTURER'S PART NO.		PLATING CONFIGURATION PER PARAGRAPH 3.1.2.2
	SOURCE 1	SOURCE 2	
2891091-01	S-1088-10	S08850845-10A	1
2891091-02	S-1088-15-5	S08850845-15	1
2891091-03		S08700870-10	1
2891091-04		S09000900-10	2
2891091-05		S08850845-10A	4
2891091-06		S09000900-10	3
2891091-07		S12451245-15G	3
2891091-08		S18451845-15	3
2891091-09		S13950645-15	3
2891091-10		S08650835-15	3
2891091-11		S21351135-15	3
2891091-12		S21351135-15	4
2891091-13		S12401240-15	3
2891091-14		S18401840-15	3

 <b>TEXAS INSTRUMENTS</b> <small>Dallas, Texas</small>	DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		A 96214		2891091	
SCALE			SHEET		9 of 9	





LOADING FIXTURE FOR 196 LEAD PACKAGE CARRIER  
 30 SEPTEMBER 1986 2437704 L. DERRYBERRY

3

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10

NOTES 1 VENDOR: BEARING, CHAIN AND SUPPLY CO.  
2221 MOCKINGBIRD LANE  
DALLAS, TEXAS 75235

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REVISIONS

REVISION

APPROVED

B-36

1	2	28	418262-16	SCREW, SKT HD, .25 LG	
1	6	27	415029-1031	.031 STK CRES ALY	
1	6	26	415029-1125	.125 STK CRES ALY	
2	2	25	415029-1125	.125 STK CRES ALY	
4	2	24	416937-15	10-32 HELICAL THD (LOCKING)	
2	2	23	416937-28	4-40 HELICAL THD (LOCKING)	
2	2	22	411197-0059	PIN, DOWEL	
1	2	21	410972-10	NUT 10-32	
1	2	20	419346-235	COMPRESSION SPRING	
2	6	19	415107-2009	.625 DIA AL ALY BAR RD	
4	2	18	419346-310	COMPRESSION SPRING	
3	2	17	419346-276	COMPRESSION SPRING	
3	2	16	41200-59	1/4 - 20 SHOULDER SCREW	
4	2	15	A-61014	BEARING PRECISION SERIES A	THOMPSON
5	2	14	418590-0012	SCREW, SKT HD, 10-32	
2	2	13	418590-0010	SCREW, SKT HD, .50 LG	
4	2	12	418262-0042	SCREW, SKT HD, .375 LG	
2	6	11	3/8 DIA X 6.0	SHAFT, CLASS 5	THOMPSON
1	5	10	415101-1050	.500 THK AL ALY AH	
1	2	9	41200-27	10-32 SHOULDER SCREW	
1	5	8	800901-38	1/2 X 6.0	
1	5	7	415101-1075	.750 THK AL ALY PL	
1	4	6	415038-2448	1 1/2 THK STAINLESS	
1	4	5	415038-2024	.750 THK CRESS BAR	
1	4	4	800901-2	1/8 X 2.00	
1	3	3	415029-1050	.05 THK CRESS SH	
1	3	2	415127-1200	2.00 THK AL ALY BAR	
1	3	1	415101-1050	.50 THK AL ALY PL	

1

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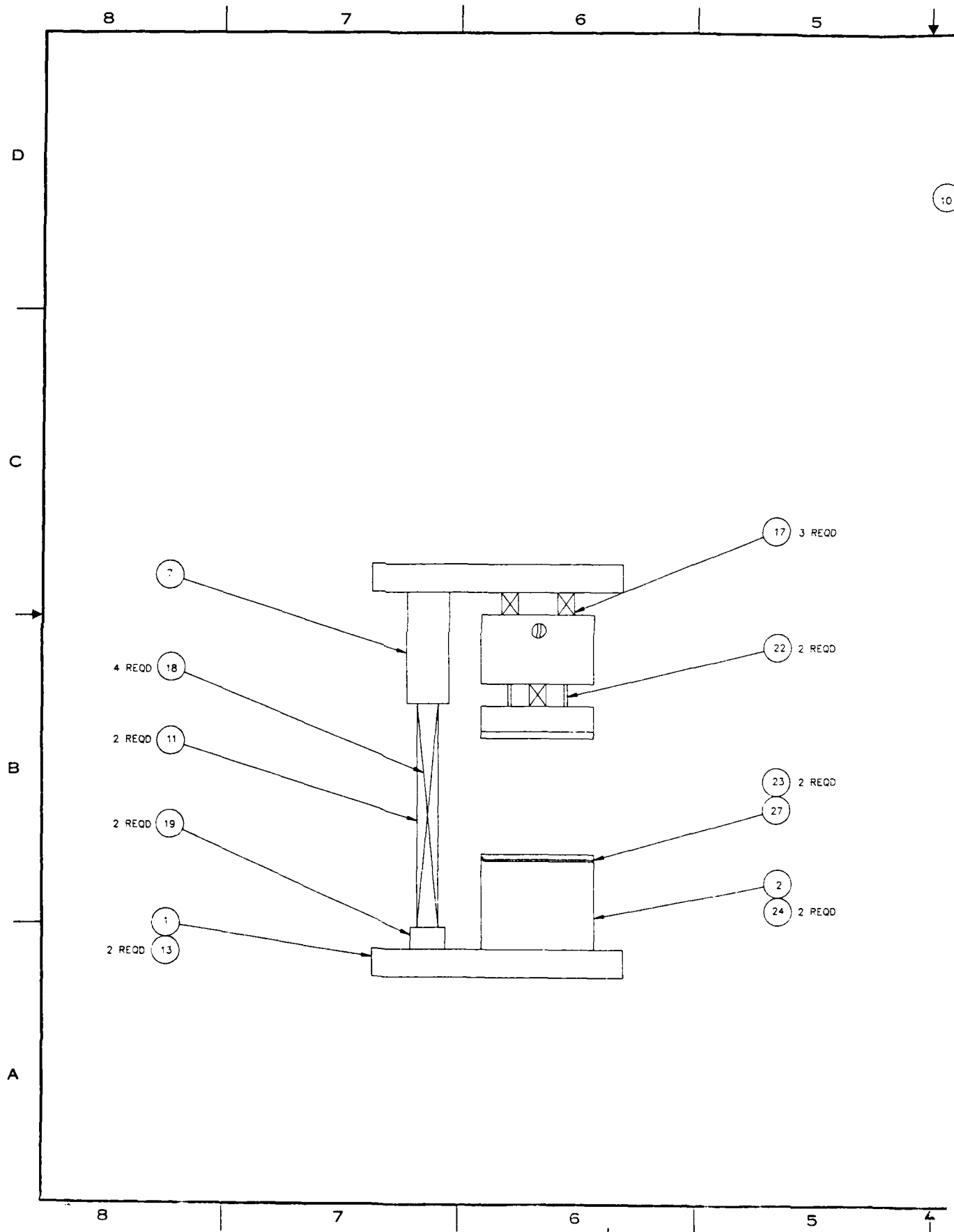
FAB	QTY	SH	DET	PART NUMBER	DESCRIPTION	SOURCE
FILED: OTHERWISE SPECIFY: * ANGLES - 1" * 1 PL DECIMALS - .010 * 2 PL DECIMALS - .02 * 1 PL DECIMALS - .08 * FRACTIONS - 1/32				TOTAL VARIATION M-A-2686134		
REV N/C				ALB/FILM DATE REV		
CHECK ENGR APPD				TEXAS INSTRUMENTS Methods Tooling		
PROJECT TOOL OWNER APPLICATION				TOOL DESCRIPTION LEAD FORM/CUT TOOL		
LENT F SPEC NO PROCESS				SCALE 1/1 DATE 7 D M-A-2686134		

4

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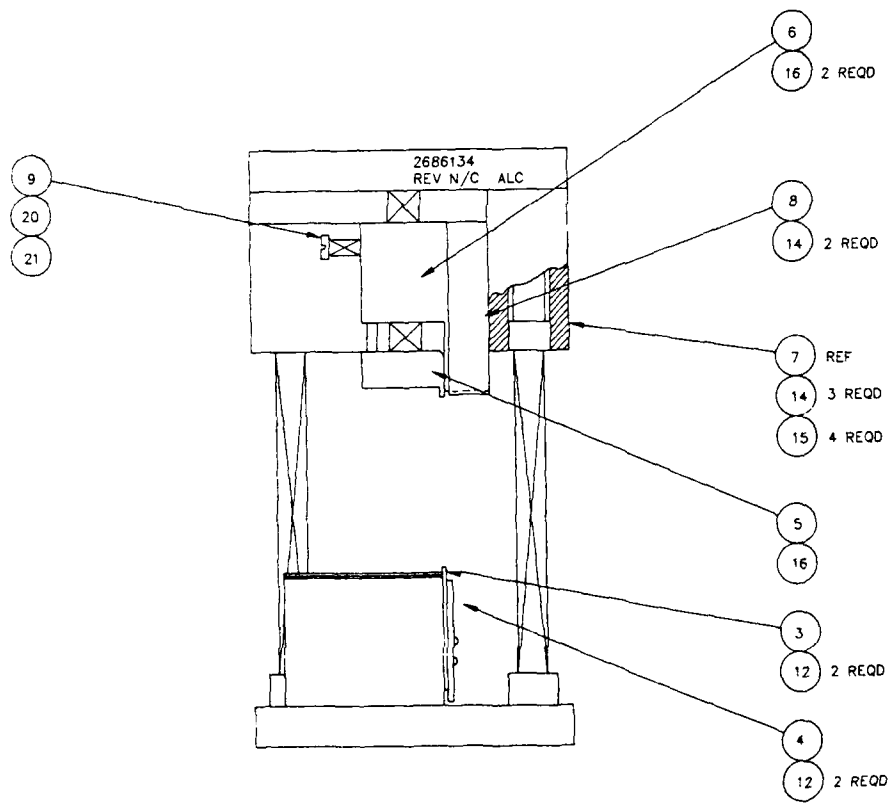
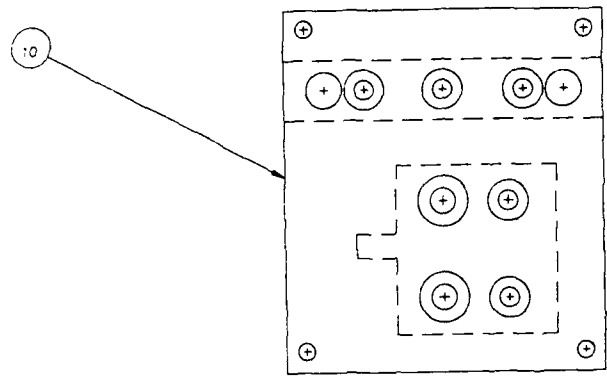
2

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4 3 1

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B-37

4 4 3 2 1

NOTES:

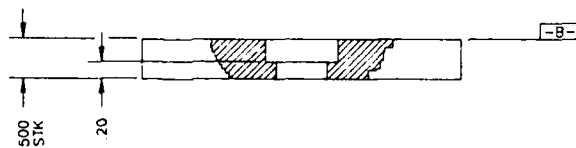
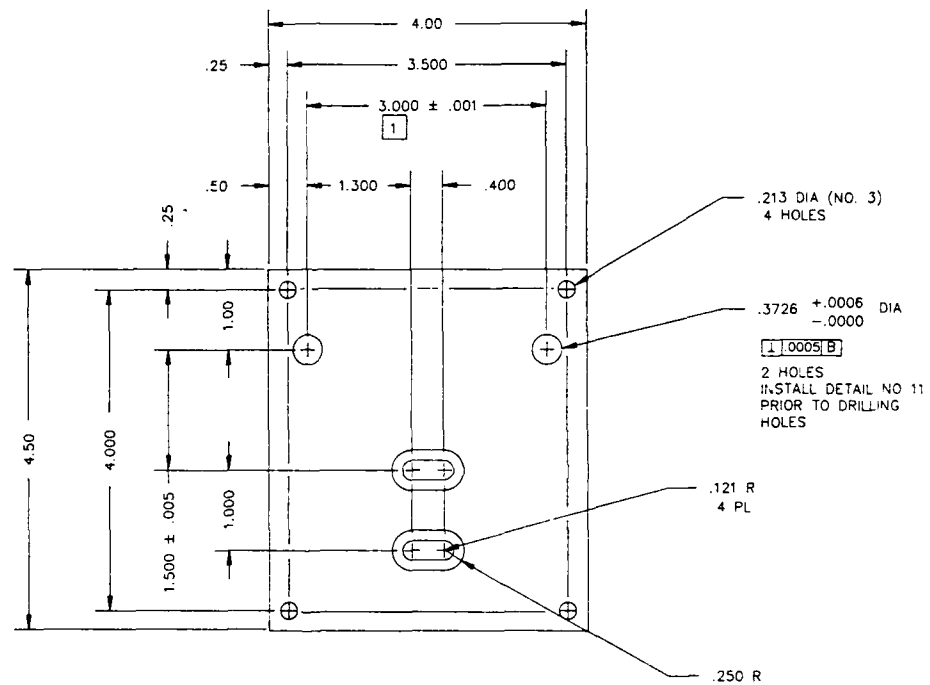
1 MATCH DRILL WITH DETAIL  
7 AND 10

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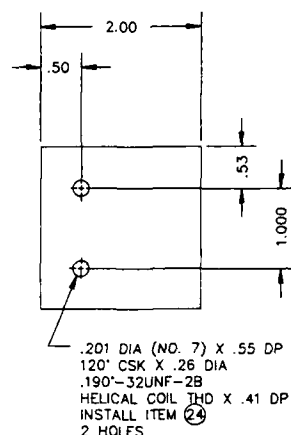
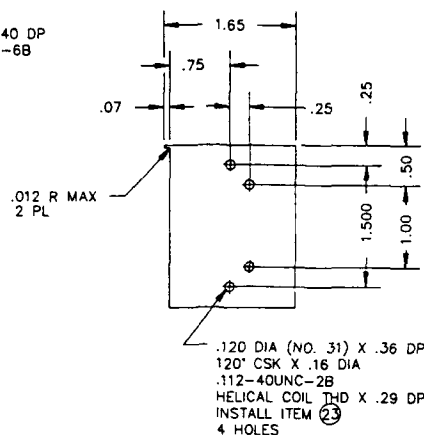
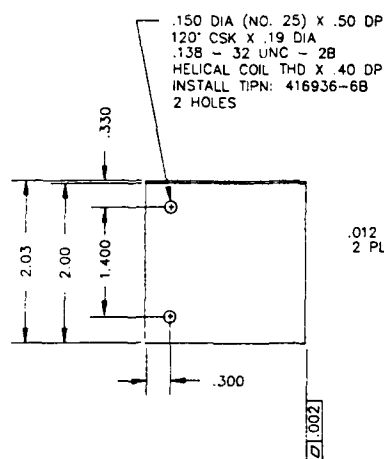
C

B

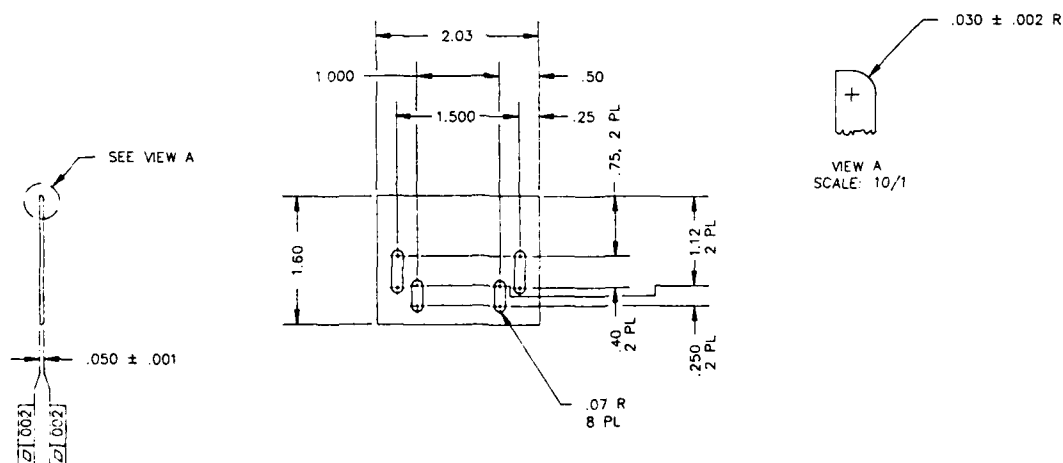
A



1	ANDZ	23-02	02G	415101-1050	500 THK AL ALY SH G081-1051
SEQ NO	IDENT	F-SPEC	NO	PART NUMBER	DESCRIPTION
	PROCESS			TOLERANCES	
INSPECTION THIS DETAIL: NOT REQD				ANGLES: 1°	
INSPECT ASSEMBLY PER EQ OPS 4.2				3 PL DIGITALS: ± .010	
ASSEMBLY TOOLING				2 PL DIGITALS: ± .02	
				1 PL DIGITAL: ± .06	
				FRACTIONAL: 1/32	
				TOOL: M-5-2.3.34	
				R.V. SCALE: 1:100 DET: 1	



1	ANDZ	23-02	02G	415127-1200	2.00 THK AL ALY BAR 6061
SEQ NO	IDENT	F-SPEC	NO	PART NUMBER	DESCRIPTION
		PROCESS		TOLERANCES	REV SCALE QTY REQ DET 2
		INSPECTION THIS DETAIL NOT REQD		ANGLES ± 1°	
		INSPECT ASSEMBLY PER EG QSP6-4-2		3 PL DECIMALS ± .010	
		ASSEMBLY TOOLING		2 PL DECIMALS ± .02	
				1 PL DECIMAL ± .06	
				FRACTIONAL ± 1/32	TOOL M-A-2686134



1	BK0XD	33-02	02G	415029-1050	B-38 .05 THK CRESS SH CLASS 304 COND A
SEQ NO	IDENT	F-SPEC	NO	PART NUMBER	DESCRIPTION
		PROCESS		TOLERANCES	REV SCALE QTY REQ DET 3
		INSPECTION THIS DETAIL NOT REQD		ANGLES ± 1°	
		INSPECT ASSEMBLY PER EG QSP6-4-2		3 PL DECIMALS ± .010	
		ASSEMBLY TOOLING		2 PL DECIMALS ± .02	
				1 PL DECIMAL ± .06	
				FRACTIONAL ± 1/32	TOOL M-A-2686134

TEXAS INSTRUMENTS	D.96214	M-A-2686134
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5

1 -IT-TR TO RC 58-60

1	2	BK0XD	33-02	02G	800901-2	1/8 X 2 A-6 TOOL STEEL					
	1	HT-TR	951-05	00		COND A					
SEQ NO		IDENT	F-SPEC	NO		PART NUMBER		DESCRIPTION			
PROCESS						TOLERANCES		REV	SCALE	QTY REQD	DET
INSPECTION THIS DETAIL: NOT REQD						ANGLES = 1"			1/1	1	4
INSPECT ASSEMBLY PER EG 05P6-4.2						3PL DECIMAL = .010					
ASSEMBLY TOOLING						2 PL DECIMAL = .02		TOOL			
						1 PL DECIMAL = .06					
						FRACTIONAL = 1/32		M-A-2686134			

1 INSTALL TIPN: 41197-0059 PRIOR  
TO DRILLING HOLE

Technical drawing of a square plate with the following dimensions and features:

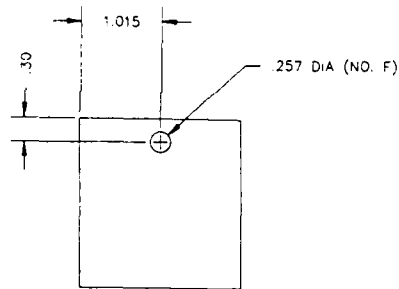
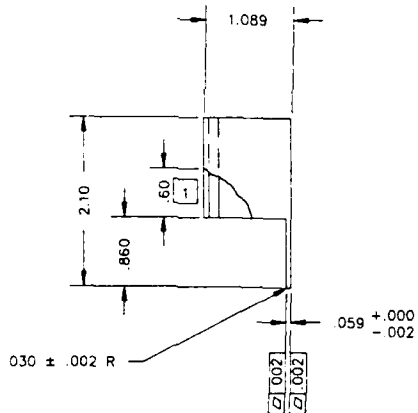
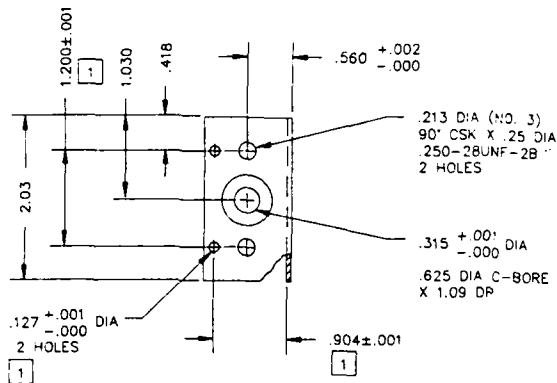
- Overall width: 2.03
- Overall height: 2.03
- Top edge: .904 ± .001
- Right edge: .500 ± .002
- Bottom edge: .1240 + .0005 / - .0000
- Left edge: .418
- Internal horizontal dimension: 1.200 ± .001
- Internal vertical dimension: 1.030
- Top right corner: .213 DIA (NO. 3) 90° CSK X .25 DIA .250-28UNF-2B
- Bottom left corner: X 15 DP 2 HOLES
- Feature 1: A square feature with a width of .1240 + .0005 / - .0000, located at the bottom left corner.
- Feature 2: A circular feature with a diameter of .213 DIA (NO. 3) 90° CSK X .25 DIA .250-28UNF-2B, located at the top right corner.
- Feature 3: A circular feature with a diameter of .213 DIA (NO. 3) 90° CSK X .25 DIA .250-28UNF-2B, located at the top center.
- Feature 4: A circular feature with a diameter of .213 DIA (NO. 3) 90° CSK X .25 DIA .250-28UNF-2B, located at the bottom center.

1	BK0X0	33-02	02G	415038-2024	750 THK CRESS BAR CLASS 304 COND A			
SFO	IDENT	F.PREC	A.U.	PART NUMBER	DESCRIPTION			
A.2	PROCESS			TOLERANCES	REV	SCALE	QTY REQD	DET
IN. SECTION THIS DIST. NOT FOLD				ANGLES 1"				(5)
IN. SECTION THIS DIST. NOT FOLD				3PL. DECIMALS - .010				
IN. SECTION THIS DIST. NOT FOLD				2 PL. DECIMALS - .02				
ASSEMBLY TOLER.				1 PL. DECIMAL - .05	707L		M4-20x3.5x14	



NOTE:

+ .001  
- .000 TOLERANCE APPLIES  
TO .60 DIM. REMINDER  
OF HOLE DIA IS  $\pm .010$



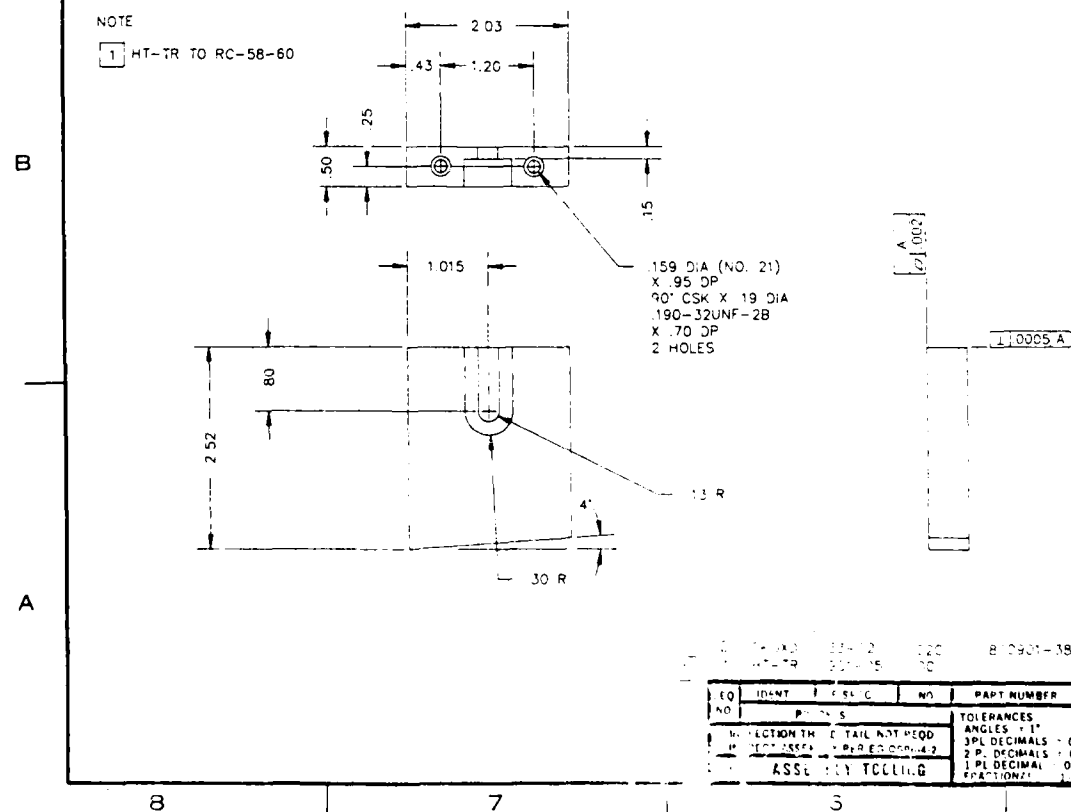
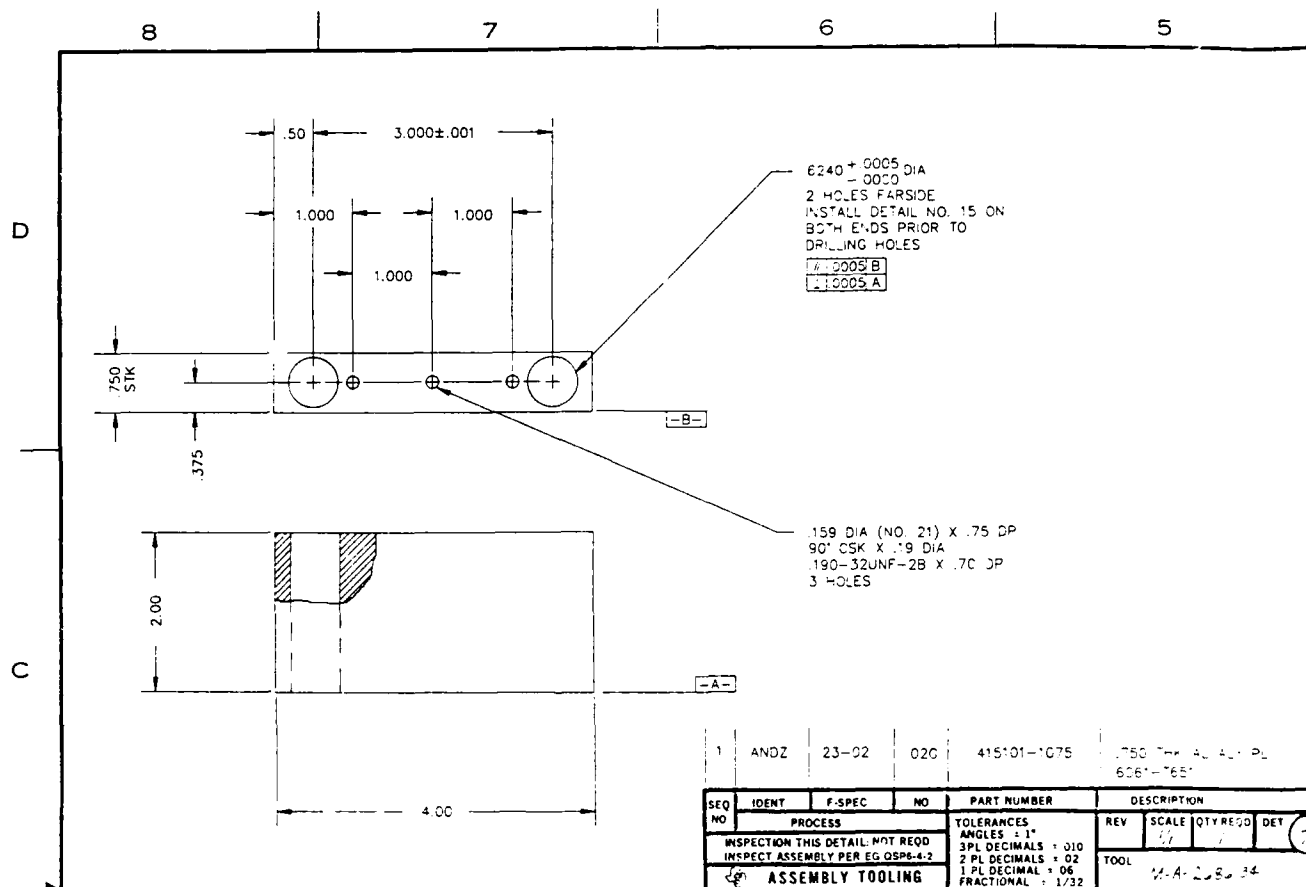
B-39

1	BK0XD	33-02	02G	415038-2448	1 1/2 THK STAINLESS STEEL BAR 304
SEQ NO	IDENT	F-SPEC	NO	PART NUMBER	DESCRIPTION
	PROCESS			TOLERANCES	REV
	INSPECTION THL. DETAIL: NOT REQD			ANGLES: 1°	SCALE
	INJECT ASST. Y PER BG 03P4-2			3 PL DECIMALS: $\pm .010$	QTY REQD
	ASSEMBLY TOOLING			2 PL DECIMALS: $\pm .02$	DET
				1 PL DECIMAL: $\pm .08$	6
				FRACTION: 1/32	
				TOOL	M-A-2686/34
					M-A-2686/34

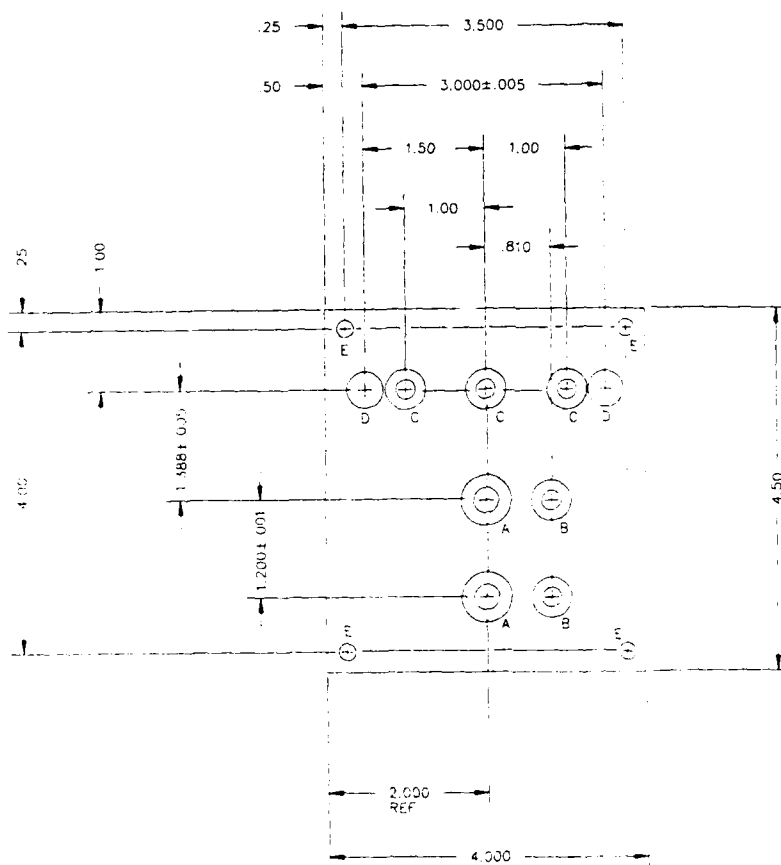
TEXAS  
INSTRUMENTS

D 96214

M-A-2686/34



LTR	HOLE DIAMETER	QTY	REMARKS
A	.215 $\pm .005$ DIA -.000 .625 DIA C-BORE X .40 DP	2	
B	.242 DIA (C) .500 DIA C-BORE X .40 DP	2	
C	.242 DIA (C) .500 DIA C-BORE X .35 DP	3	
D	.453 DIA (29164)	2	
E	.213 (1.0. 3)	4	



B-40

2. HOLE DIA .215 ± .005 (1.0. 3) HOLE DIA .215 ± .005 (1.0. 3) HOLE DIA .215 ± .005 (1.0. 3)

SEC	IDENT	REV	SCALE	QTY	REQD	DET
1	1.00	1.00	1.00	1.00	1.00	1.00
2	1.00	1.00	1.00	1.00	1.00	1.00
3	1.00	1.00	1.00	1.00	1.00	1.00
4	1.00	1.00	1.00	1.00	1.00	1.00
5	1.00	1.00	1.00	1.00	1.00	1.00
6	1.00	1.00	1.00	1.00	1.00	1.00
7	1.00	1.00	1.00	1.00	1.00	1.00
8	1.00	1.00	1.00	1.00	1.00	1.00
9	1.00	1.00	1.00	1.00	1.00	1.00
10	1.00	1.00	1.00	1.00	1.00	1.00

TEXAS INSTRUMENTS

D51214

A

3/8 DIA X 6.0 L      1 SHAFT, THOMPSON  
CLASS 5

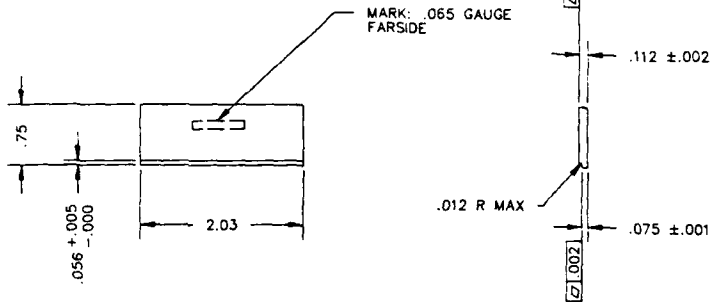
SEQ NO	IDENT	F-SPEC	NO	PART NUMBER	DESCRIPTION
	PROCESS			TOLERANCES	REV
INSPECTION THIS DETAIL: NOT REQD INSPECT ASSEMBLY PER EG OSP#4-2				ANGLES = 1°	SCALE 1/1
				3 PL DECIMALS = 010	QTY REQD 2
				2 PL DECIMALS = 02	DET 1
				1 PL DECIMAL = 06	
ASSEMBLY TOOLING				FRACTIONAL = 1/32	TOOL M-A-268-134

1	ANDZ	23-02	000	41107 0029	625 DIA AL ALY BAR RD 6061 -H31
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SEQ NO	IDENT	P-SPEC	PART NUMBER	DESCRIPTION
	PROCESS			
	INSPECTION THIS DETAIL: NOT R		TOLERANCES	REV
	EFFECT ASSEMBLY PER ECD		ANGLES 1P	SCALE 10:1
			171 DEC AL 010	DET
			2 PLD 01 AL 02	
			1 F 0 AL 06	TOOL
			1/32	M. - 2. 2. 3d
	ASSEMBLY TOOLIN			

NOTES: 1 HGT .12, (CAT 4)



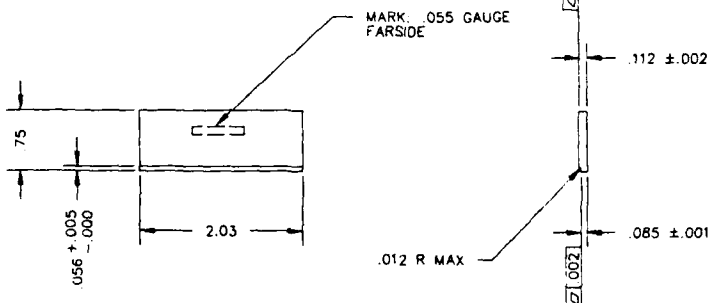
AFT. THOMPSON  
ASS 5

DESCRIPTION	SCALE	QTY REQD	DET
	2		11
M-A-2686134			

2	MARK	902-01	01G	415029-1125	.125 THK CRESS ALY SH
1	BK0XD	33-02	02G		304 ANL

SEQ NO	IDENT	F-SPEC	NO	PART NUMBER	DESCRIPTION
1	PROCESS				
INSPECTION THIS DETAIL: NOT REQD				TOLERANCES	REV
INSPECT ASSEMBLY PER EG QSPS-4-2				ANGLES ± 1°	SCALE
ASSEMBLY TOOLING				3 PL DECIMALS ± .010	QTY REQD
				2 PL DECIMALS ± .02	DET
				1 PL DECIMAL ± .06	25
				FRACTIONAL ± 1/32	TOOL
					M-A-2686134

NOTES: 1 HGT .12, (CAT 4)



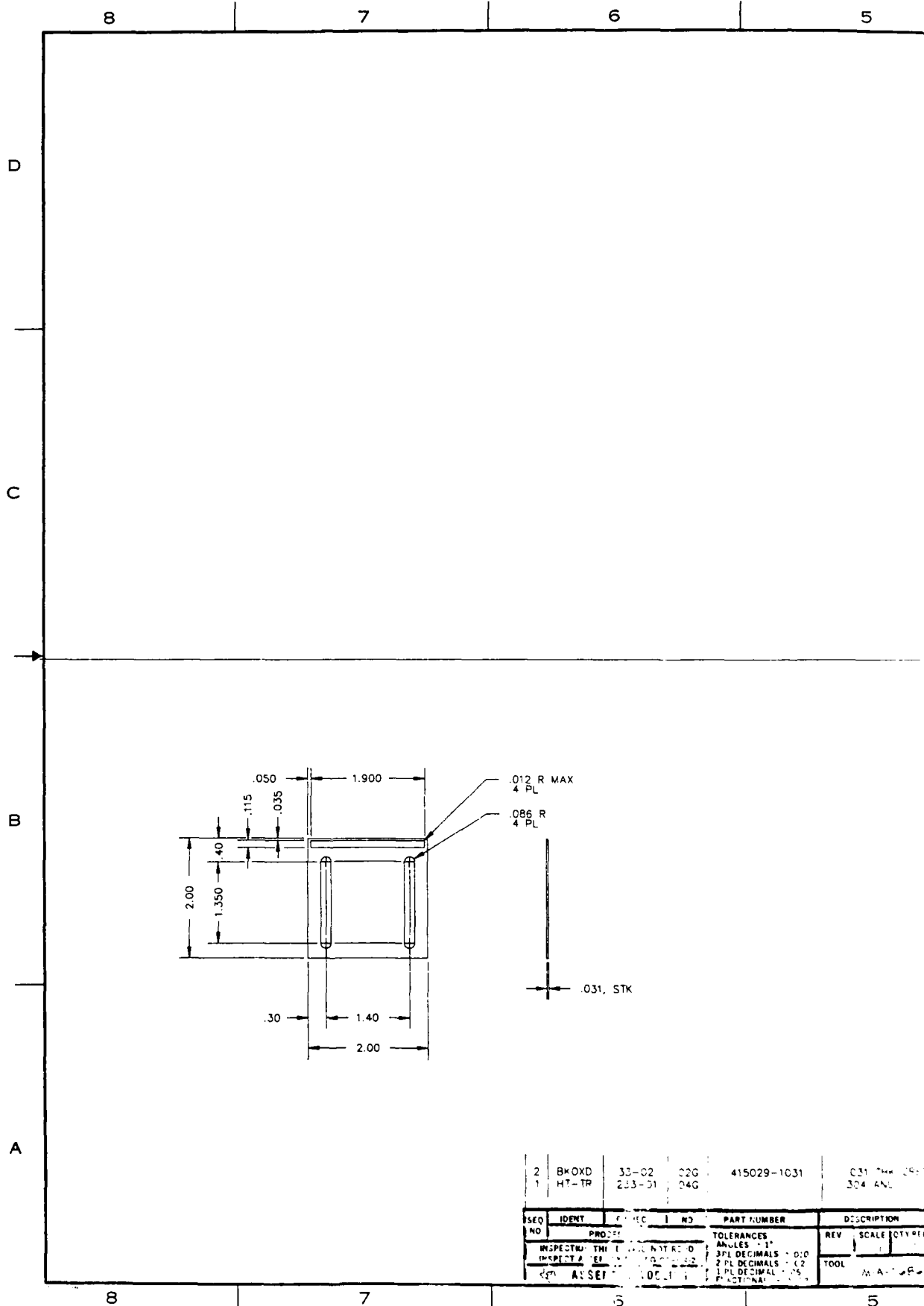
A PL ALY HAW PL  
M-A-2686134

DESCRIPTION	SCALE	QTY REQD	DET
	2		13
M-A-2686134			

1	2	MARK	902-01	01G	415029-1125	.125 THK CRESS ALY SH
	1	BK0XD	33-02	02G		304 ANL

SEQ NO	IDENT	F-SPEC	NO	PART NUMBER	DESCRIPTION
1	PROCESS				
INSPECTION THIS DETAIL: NOT REQD				TOLERANCES	REV
INSPECT ASSEMBLY PER EG QSPS-4-2				ANGLES ± 1°	SCALE
ASSEMBLY TOOLING				3 PL DECIMALS ± .010	QTY REQD
				2 PL DECIMALS ± .02	DET
				1 PL DECIMAL ± .06	26
				FRACTIONAL ± 1/32	TOOL
					M-A-2686134

INSPECTION	D 96214	M-A-2686134
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4 3 1

D

C

B

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INK PRESS 411

OPTION		
FILE	QTY	REQD DET
1		(21)

411 86134

B-42

IN	FILE	D 96214	N-A 2484134	7
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4 3 2 1

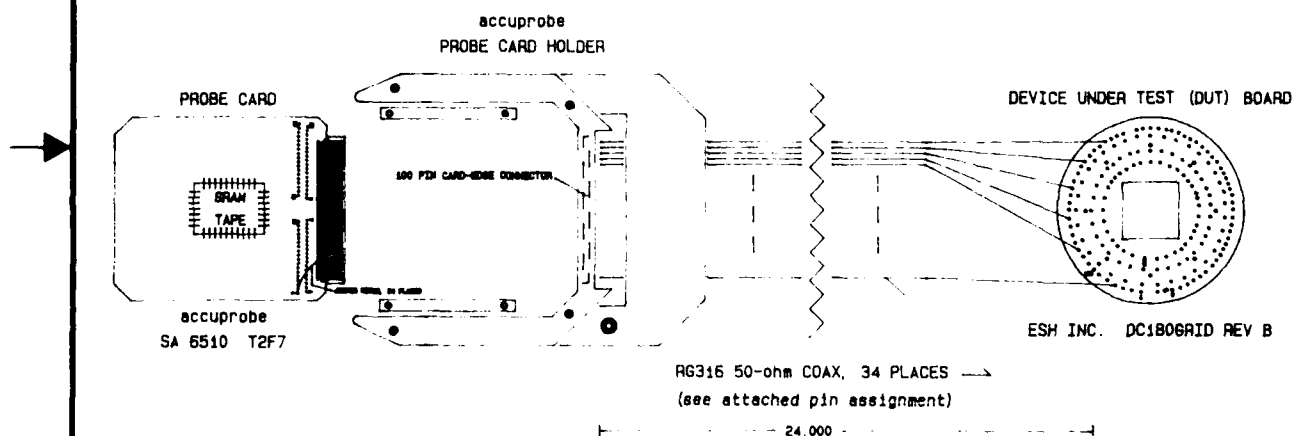
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APPENDIX C  
ADDITIONAL ELECTRICAL DIAGRAMS

<u>Page</u>	<u>Drawing Number</u>	<u>Document</u>
C-2 - C-5	2437688	Single-chip SRAM to DUT Board Assembly
C-6 - C-9	2437689	SRAM Substrate to DUT Card Assembly
C-10 - C-13	2437690	Socket on DUT Board Assembly
C-14 - C-15	2437691	Power Analysis Test Fixture
C-16 - C-18	2437707	X4 SRAM Package Pin Assignment



# LABCOM SINGLE CHIP SRAM TO DUT BOARD ASSEMBLY



<p>TEXAS INSTRUMENTS INCORPORATED Dallas, Texas</p>	DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		A	96214	2437688	
			SCALE		SHEET 1	

DWG NO

2437688

SH 2

## LABCOM

## SRAM - SINGLE CHIP PROBE CARD-TO-DUT BOARD PIN ASSIGNMENT

Signal Name	Probe No.	Card-edge Connector	DUT Board Pin No.
VDD	1	17	46s/44f
GND			GND
A4	2	19	5
GND			GND
A5	3	21	4
GND			GND
A6	4	23	3
GND			GND
A7	5	25	1
GND			GND
A8	6	27	20
GND			GND
/RST	7	29	119
GND			GND
/CS	8	31	15
GND			GND
CLK/WE	9	33	9
GND			GND
CT2	10	35	10
GND			GND
CT1	11	37	24
GND			GND
CT0	12	39	26
GND			GND
A3	13	41	2
GND			GND
A2	14	43	8
GND			GND
A1	15	45	7
GND			GND

TEXAS  
INSTRUMENTS  
Dallas, Texas

DWN

DATE

SIZE

FSCM NO

DRAWING NO

REV

A

96214

2437688

ISSUE DATE

SCALE

SHEET

2

DWG NO

2437688

SH 3

Signal Name	Probe No.	Card-edge Connector	DUT Board Pin No.
/PV GND	16	47	50 GND
A0 GND	17	49	6 GND
VSS GND	18	51	56/57 GND
VSS GND	20	53	56/57 GND
VCC GND	21	55	43 GND
A11 GND	22	57	18 GND
A12 GND	23	59	19 GND
DQ0 GND	24	61	11/12 GND
DQ1 GND	25	63	13/14 GND
DQ2 GND	26	65	27/28 GND
DQ3 GND	27	67	29/30 GND
DQ8/P GND	29	69	39/40 GND
DQ7 GND	30	71	37/38 GND
DQ6 GND	31	73	35/36 GND
DQ5 GND	32	75	33/34 GND
DQ4 GND	33	77	31/32 GND



**TEXAS**  
INSTRUMENTS  
Dallas, Texas

DWN

DATE

SIZE

FSCM NO

**A****96214**

DRAWING NO

2437688

REV

ISSUE DATE

SCALE

SHEET 3

DWG NO 2437688 SH 4

Signal Name	Probe No.	Card-edge Connector	DUT Board Pin No.
A10 GND	34	79	17 GND
A9 GND	35	81	16 GND
VDD GND	36	83	46s/44f GND



DWN DATE  
ISSUE DATE

SIZE FSCM NO  
**A 96214**

DRAWING NO 2437688

REV

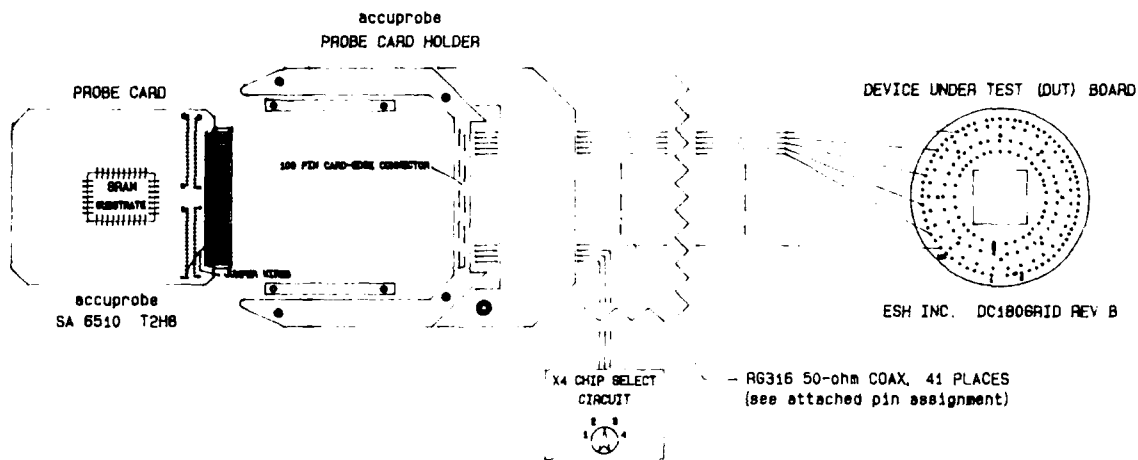
SCALE


SHEET 4

DWG NO 2437689

SH 1

# LABCOM SRAM SUBSTRATE TO DUT CARD ASSEMBLY



 <b>TEXAS INSTRUMENTS</b> <small>INCORPORATED</small> <small>Dallas, Texas</small>	DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		A	96214	2437689	
			SCALE		SHEET	1


11-70108

C-6

LABCOM

SRAM - X4 CHIP PROBE CARD-TO-DUT BOARD PIN ASSIGNMENT

Signal Name	Probe No.	Card-edge Connector	DUT Board Pin No.
VDD	8	17	44
	W	83	46
	28		
	RR		
A4	23	19	5
A5	Z	21	4
A6	22	23	3
A7	21	25	1
A8	X	27	20
/RST	P	29	119
/CS	To Select Circuit Card-edge pin 6		15
CLK/WE	12	33	9
CT2	T	35	10
CT1	16	37	24
CT0	17	39	26
A3	AA	41	2
A2	BB	43	8
A1	25	45	7
/PV	15	47	50
	14		
	R		
	13		
A0	CC	49	6

 <b>TEXAS INSTRUMENTS</b> <small>Dallas, Texas</small>	OWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		A	96214	2437689	
			SCALE		SHEET	2

DWG NO

2437689

SH 3

Signal Name	Probe No.	Card-edge Connector	DUT Board Pin No.
VSS	4	51	56
	6	53	57
	11		
	S		
	24		
	26		
	30		
VCC	LL		
	B	55	43
	7		
	9		
	U		
	Y		
	27		
A11	29		
	35		
A12	18	57	18
DQ0/DQ9	V	59	19
	31	61	11/12
DQ1/DQ10	A		
	KK	63	13/14
DQ2/DQ11	I		
	32	65	27/28
DQ3/DQ12	2		
	33	67	29/30
DQ8/P/DQ17/P	C		
	36	69	39/40
DQ7/DQ16	F		
	PP	71	37/38
DQ6/DQ15	5		
	NN	73	35/36
DQ5/DQ14	E		
	34	75	33/34
DQ4/DQ13	D		
	MM	77	31/32
	3		

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INSTRUMENTS  
Da as Texas

OWN

DATE

SIZE

FSCM NO

A

96214

DRAWING NO

2437689

REV

ISSUE DATE

SCALE

SHEET 3

C-8

DWG NO

2437689

SH 4

Signal  
NameProbe  
No.Card-edge  
ConnectorDUT Board  
Pin No.

A10

19

79

17

A9

20

81

16

## X4 Select Circuit Wiring

VCC (+5)

From Card-edge  
Connector Pin 55

2

VSS (GROUND)

From Card-edge  
Connector Pin 51/53

4

CS/

From Card-edge  
Connector Pin 31

6

CS1/

N

8

N/A

CS2/

M

10

N/A

CS3/

10

12

N/A

CS4/

L

14

N/A

NOTE: Use shielded cable for all CS/ lines.



OWN

DATE

SIZE

PSCM NO

DRAWING NO

REV

A

96214

2437689

ISSUE DATE

SCALE

SHEET 4

C-9

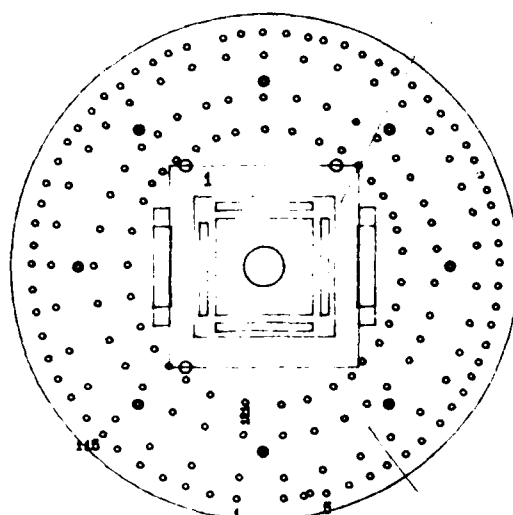
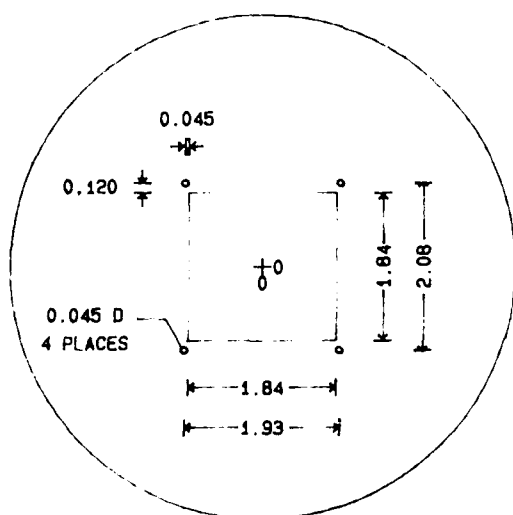


DWG NO 2437690

SH 1

# LABCOM SOCKET ON DUT BOARD ASSEMBLY

SOCKET: 3M/TEXTOL 2XX-6583 →



DEVICE UNDER TEST (DUT) BOARD: →  
ESH INC. DC180GRID REV B

 <b>TEXAS INSTRUMENTS</b> <small>INCORPORATED</small> <small>Dallas, Texas</small>	OWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		A	96214	2437690	
			SCALE		SHEET	1

C-10

DWG NO

2437690

SH 2

## LABCOM

## SRAM - X4 PACKAGE/SOCKET-TO-DUT BOARD PIN ASSIGNMENT

Signal Name	Package/Socket Pin No.	DUT Board Pin No.
VSS	9	56
	41	57
	58	
	90	
	107	
	139	
	156	
	188	
VCC	17	43
	33	
	66	
	82	
	115	
	131	
	164	
	180	
VDD	25	44
	74	46
	123	
	172	
DQ0/DQ9	3	11
	29	12
DQ1/DQ10	5	13
	31	14
DQ2/DQ11	7	27
	34	28
DQ3/DQ12	10	29
	36	30
DQ4/DQ13	12	31
	38	32
DQ5/DQ14	14	33
	40	34
DQ6/DQ15	16	35
	43	36

TEXAS  
INSTRUMENTS  
Dallas, Texas

DWN

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FSCM NO

A

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SCALE

SHEET 2

C-11

DWG NO

2437690

SH 3

Signal  
NamePackage/Socket  
Pin No.DUT Board  
Pin No.

DQ7/DQ16

19  
4537  
38

DQ8/P/DQ17/P

21  
4739  
40

/CS

N/A

15

(To chip select circuit)

/CS4

85  
(From chip select circuit)

N/A

/CS3

87  
(From chip select circuit)

N/A

/CS2

89  
(From chip select circuit)

N/A

/CS1

92  
(From chip select circuit)

N/A

CLK/WE

94

9

/RST

47 or 119

/PV4

102

50

/PV3

104

50

/PV2

106

50

/PV1

109

50

CT2

111

10

CT1

113

24

CT0

116

26

A12

118

19

A11

120

18

A10

122

17

A9

125

16


**TEXAS**  
**INSTRUMENTS**  
Dallas, Texas

OWN

DATE

SIZE

FSCM NO

**A****96214**

DRAWING NO

2437690

REV

ISSUE DATE

SCALE

SHEET 3

C-12

DWG NO

2437690

SH 4

Signal  
NamePackage/Socket  
Pin No.DUT Board  
Pin No.

A8	127	20
A7	129	1
A6	132	3
A5	134	4
A4	136	5
A3	138	2
A2	141	8
A1	143	7
A0	145	6

**TEXAS  
INSTRUMENTS**  
Dallas, Texas

DWN DATE

ISSUE DATE

SIZE

FSCM NO

**A****96214**

DRAWING NO

2437690

REV

SCALE

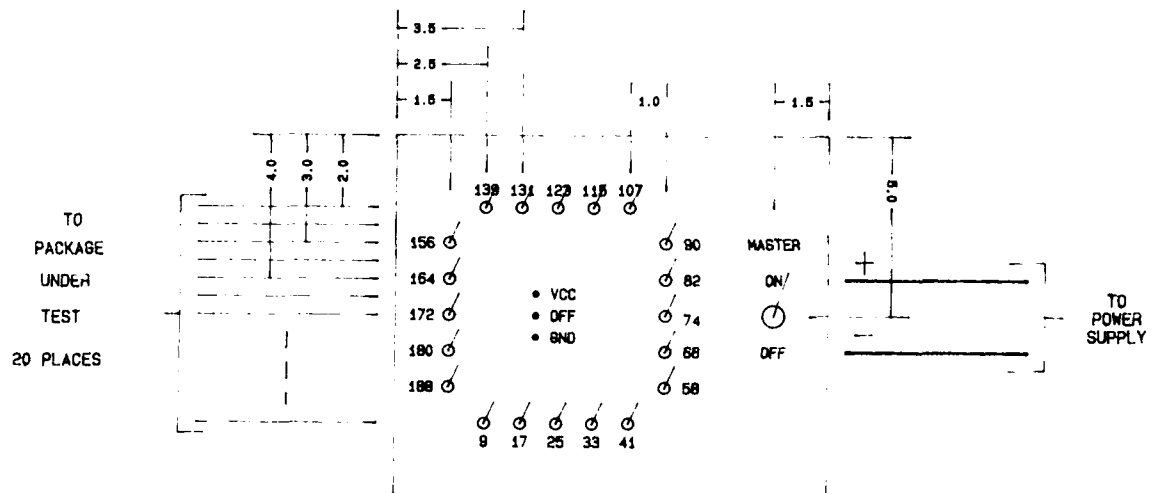
SHEET 4

C-13


DWG NO 2437691

SH 1

POWER ANALYSIS TEST FIXTURE



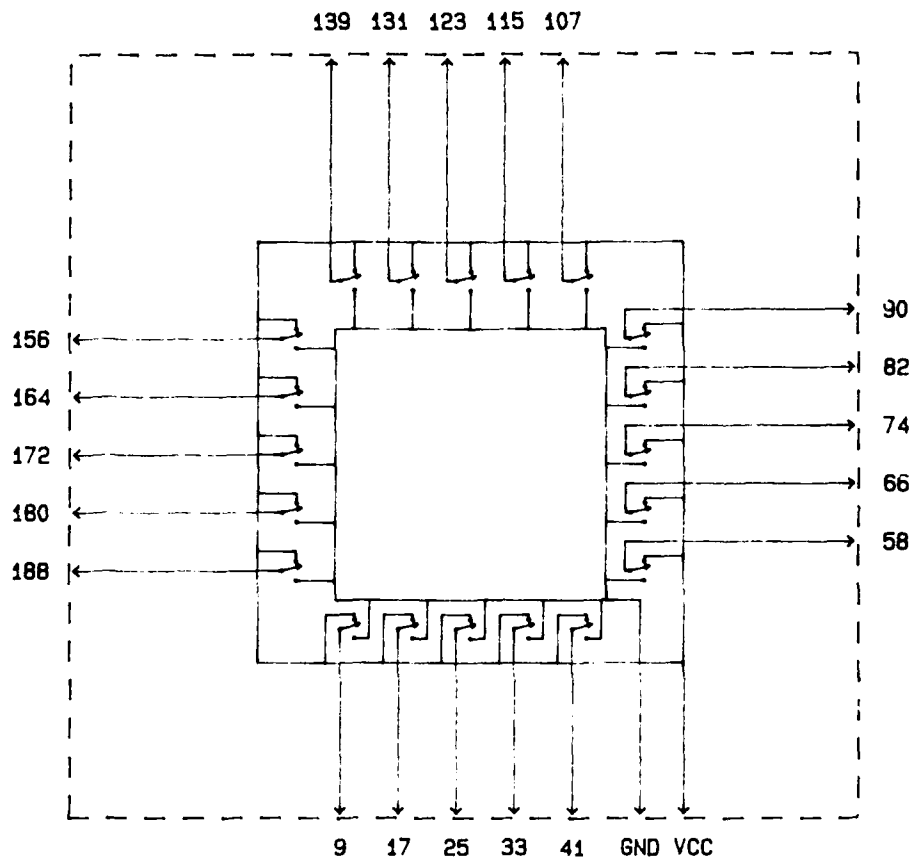
10X12X3 BUD CHASSIS

 TEXAS INSTRUMENTS INCORPORATED Dallas, Texas	OWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		A	96214	2437691	
			SCALE		SHEET 1	

71 19188

C-14


# POWER ANALYSIS TEST FIXTURE



 <b>TEXAS INSTRUMENTS</b> <small>INCORPORATED</small> <i>Dallas, Texas</i>	DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		A	96214	2437691	
			SCALE	SHEET 2		

LABCOM - VMC  
X4 SRAM PACKAGE PIN ASSIGNMENT

Signal Name	Package Pin No.
VSS	9
	41
	58
	90
	107
	139
	156
VSS	188
VCC	17
	33
	66
	82
	115
	131
	164
VCC	180
VDD	25
	74
	123
VDD	172
DQ0	3
DQ1	5
DQ2	7
DQ3	10
DQ4	12
DQ5	14
DQ6	16
DQ7	19
DQ8/P	21

 <b>TEXAS INSTRUMENTS</b> <small>Dallas, Texas</small>	DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		A 96214		2437707	
SCALE					SHEET 1	

DWG NO 2437707 SH 2

Signal  
Name

Package  
Pin No.

DQ9	29
DQ10	31
DQ11	34
DQ12	36
DQ13	38
DQ14	40
DQ15	43
DQ16	45
DQ17	47
/CS4	85
/CS3	87
/CS2	89
/CS1	92
CLK/WE	94
/RST	96
/PV4	102
/PV3	104
/PV2	106
/PV1	109
CT2	111
CT1	113
CT0	116

 **TEXAS**  
**INSTRUMENTS**  
Dallas, Texas

DWN

DATE

SIZE

FSCM NO

DRAWING NO

REV

**A**

**96214**

2437707

ISSUE DATE

SCALE

SHEET 2

C-17



DWG NO 2437707

SH 3

Signal  
NamePackage  
Pin No.

A12	118
A11	120
A10	122
A9	125
A8	127
A7	129
A6	132
A5	134
A4	136
A3	138
A2	141
A1	143
A0	145

 **TEXAS  
INSTRUMENTS**  
Dallas, Texas

DWN

DATE

SIZE

FSCM NO

**A****96214**

DRAWING NO

2437707

REV

ISSUE DATE

SCALE

SHEET 3

APPENDIX D  
PROCESSING EQUIPMENT PHOTOGRAPHS

<u>Page</u>	<u>TI Photo Number</u>	<u>Description</u>
D-2	1009-52	Magnatron MRC903 Sputter System
D-2	1009-47	Verco Probe & Tencor Alpha Profilometer
D-3	1009-53	Zicon Series 10000 Autocoater
D-3	1009-50	Cannon PLA501F Printer
D-4	1009-49	Infrared Scope & IMI Bump Plater
D-4	1009-55	Microscience Plasmalab Reactor
D-5	1009-51	Microautomation Dicing Saw
D-5	1009-42	IMI 1207 Bonder
D-6	1009-48	Dage Microtester 22 Bond Tester
D-6	1009-44	IMI Lead Forming Tool and Tape
D-7	0099-24	Firing Furnaces
D-7	0099-35	K&S Bonders
D-8	181-334	Screen Printer
D-8	0099-31	Laser Scribe



Figure D-1. Magnatron MRC903 sputter system.

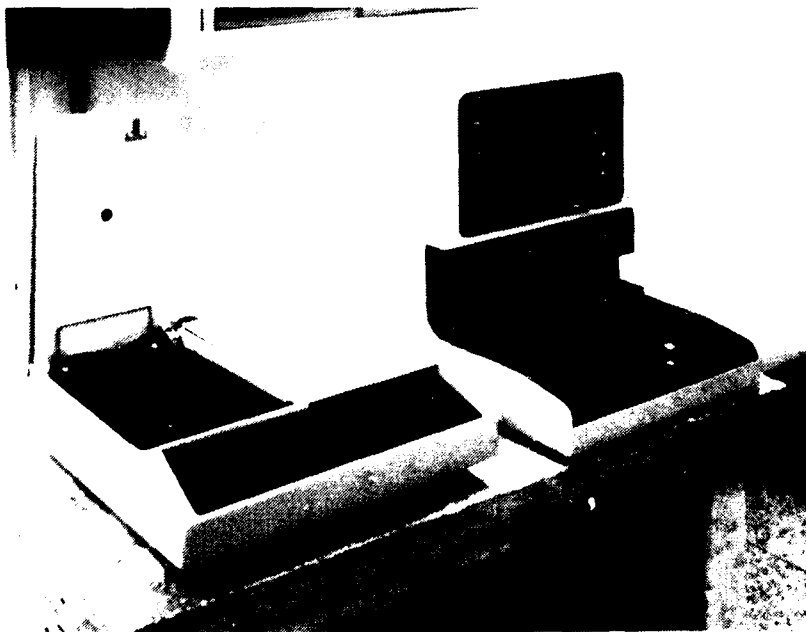


Figure D-2. Verco probe and Tencor Alpha profilometer.

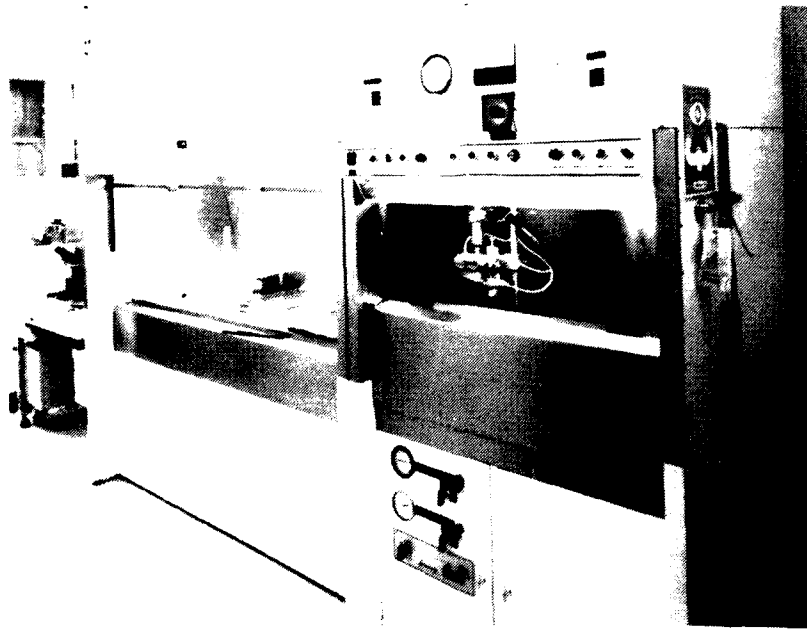


Figure D-3. Zicon Series 10000 autocoater.



Figure D-4. Canon PLA 501F printer.

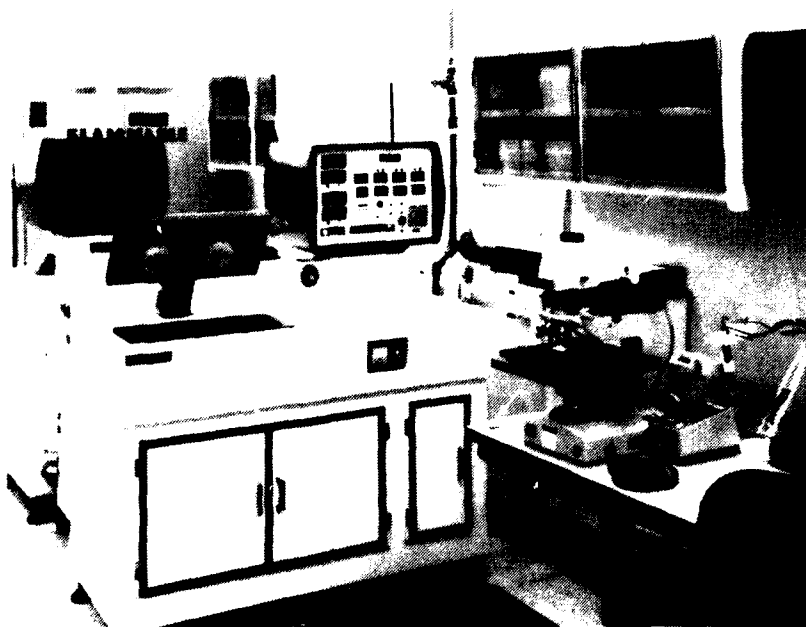


Figure D-5. Infrared scope and IMI bump plater.



Figure D-6. Microscience Plasmalab reactor.

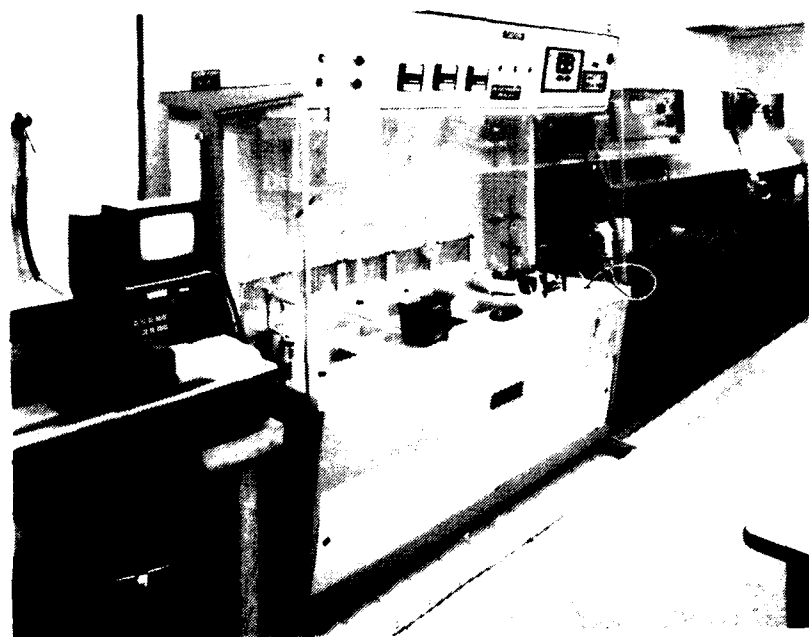


Figure D-7. Microautomation dicing saw.

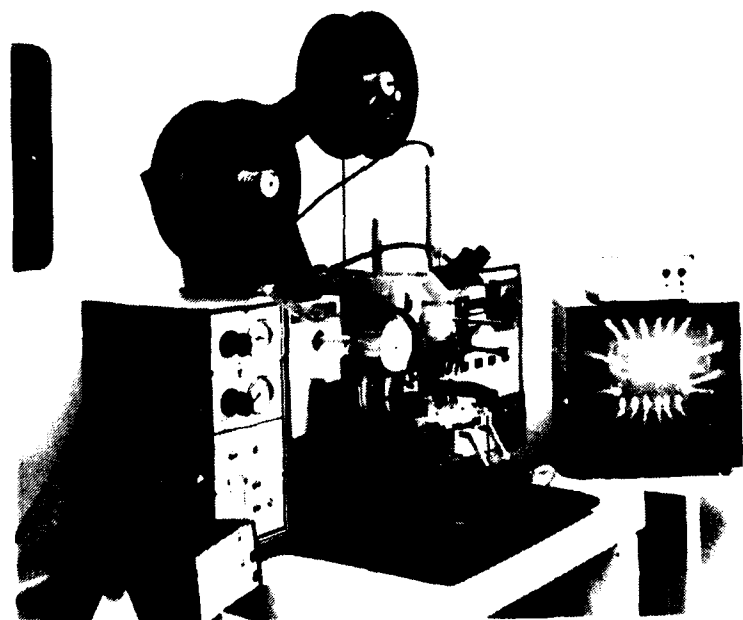


Figure D-8. IMI 1207 bonder.

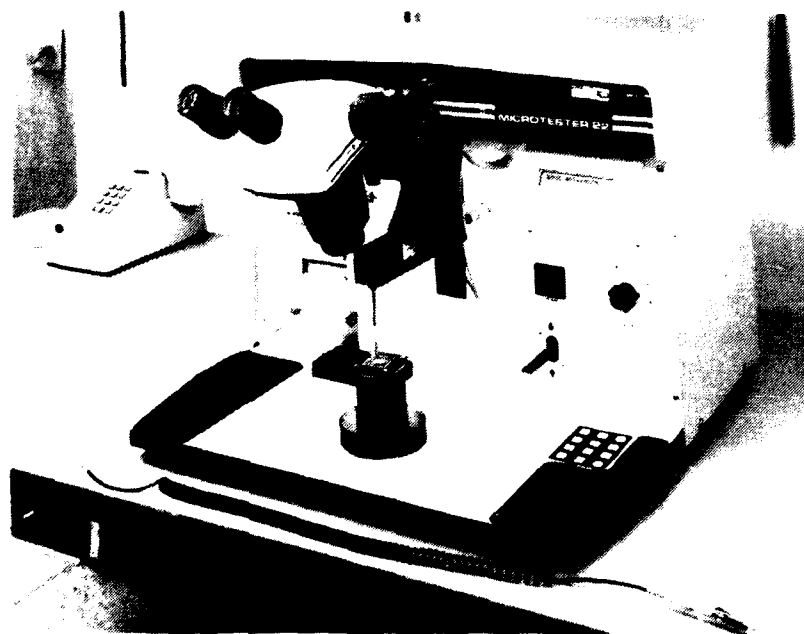


Figure D-9. Page Microtester 20 bond tester.



Figure D-10. IMI lead forging tool and types.

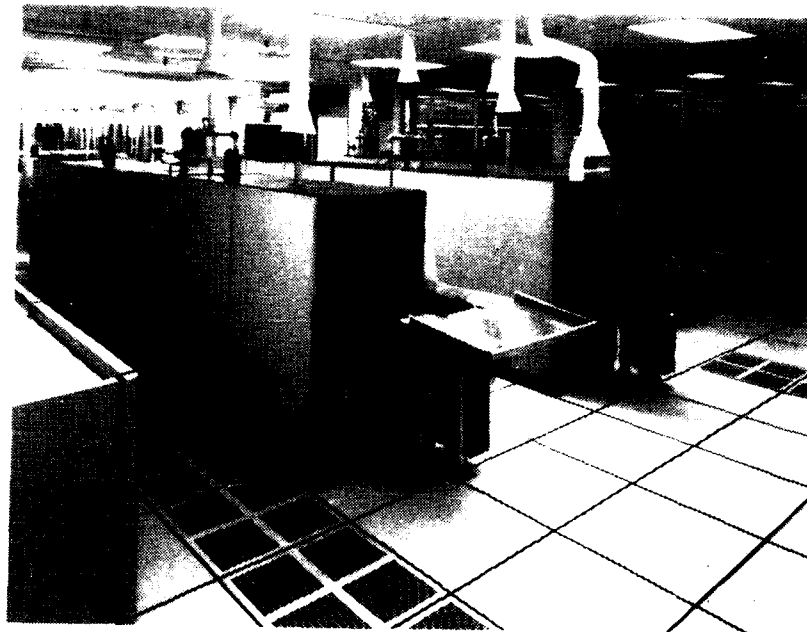


Figure D-11. Firing furnaces.



Figure D-12. K&S bonders.



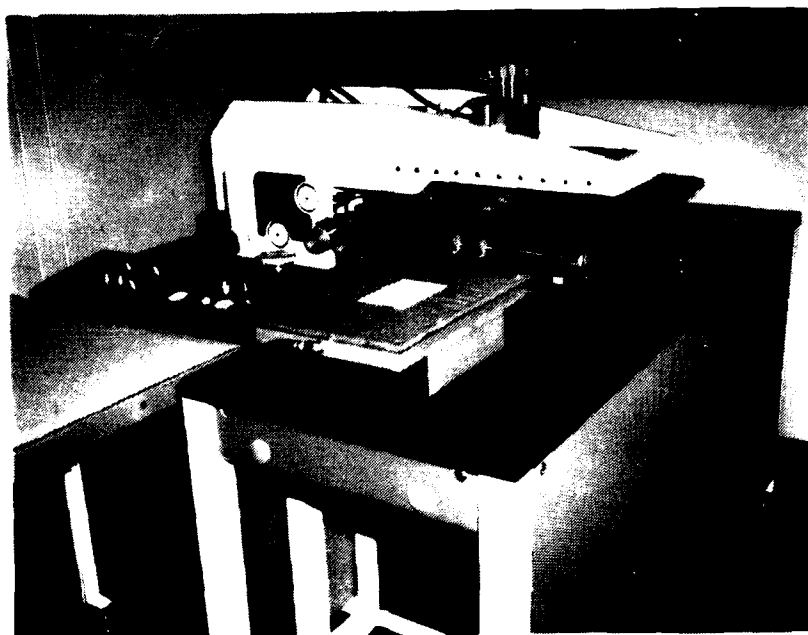


Figure D-13. Screen printers.

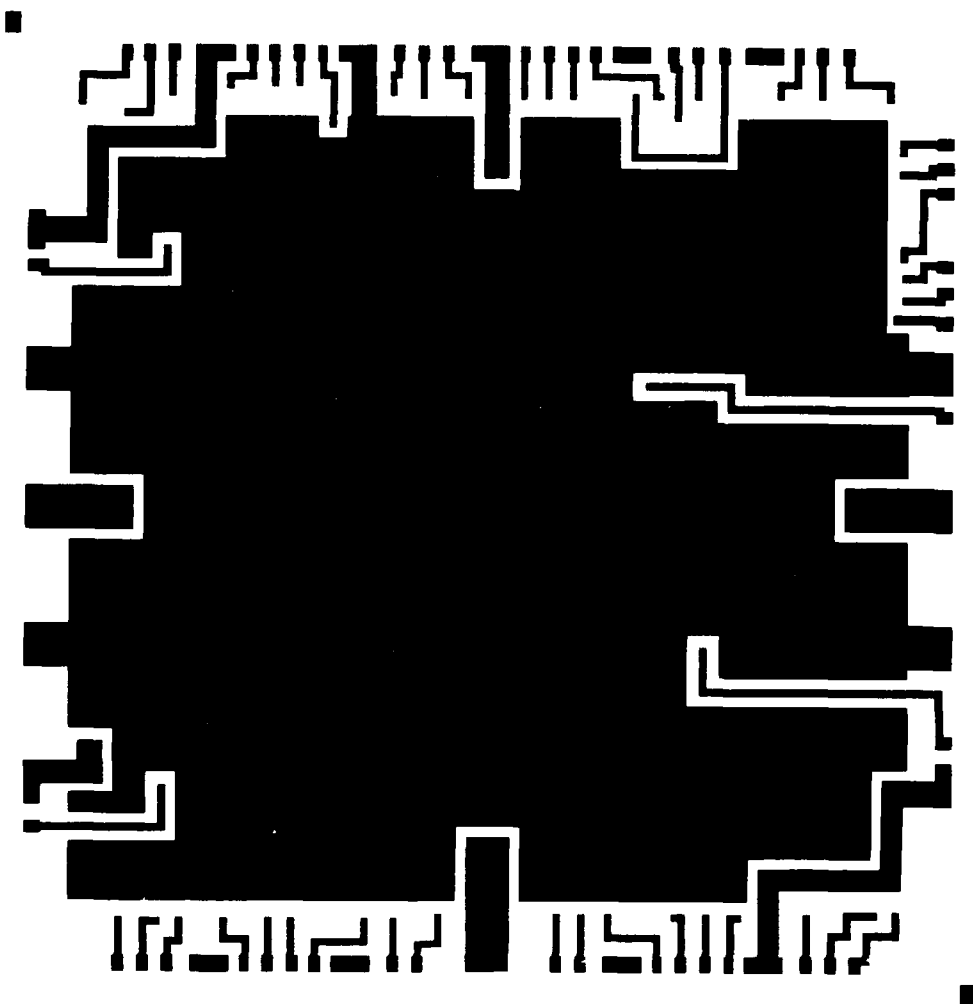


Figure D-14. Laboratory.

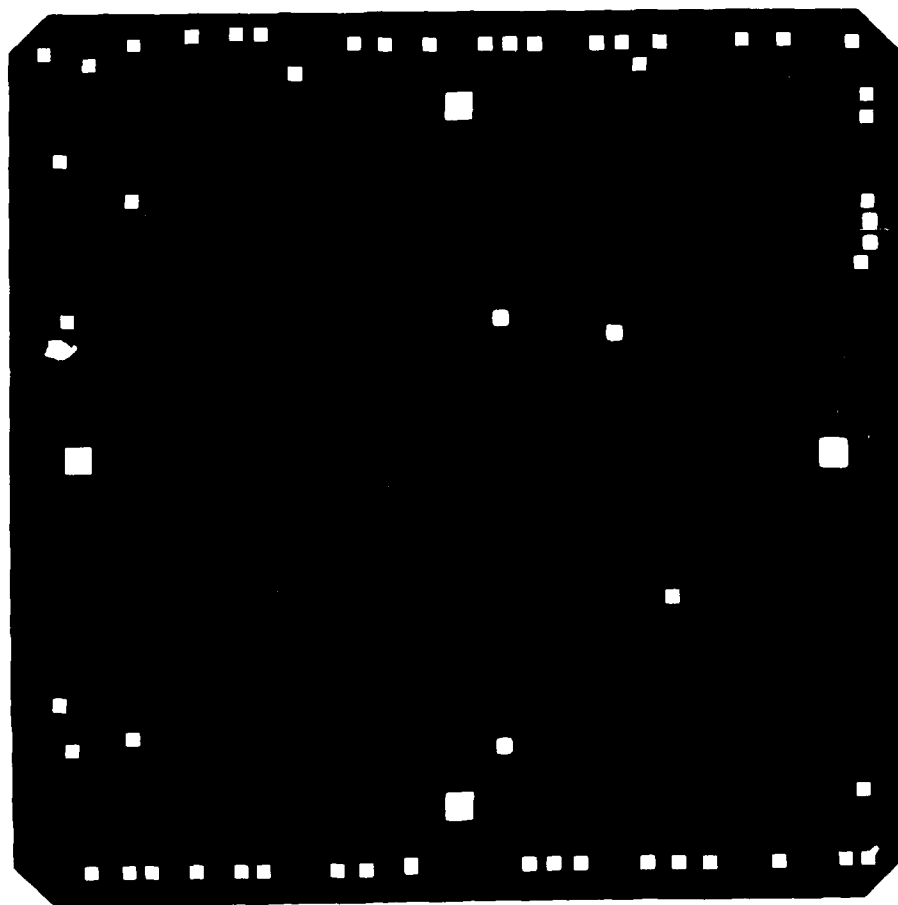
# APPENDIX E

## TEXAS INSTRUMENTS THICK FILM INTERCONNECT

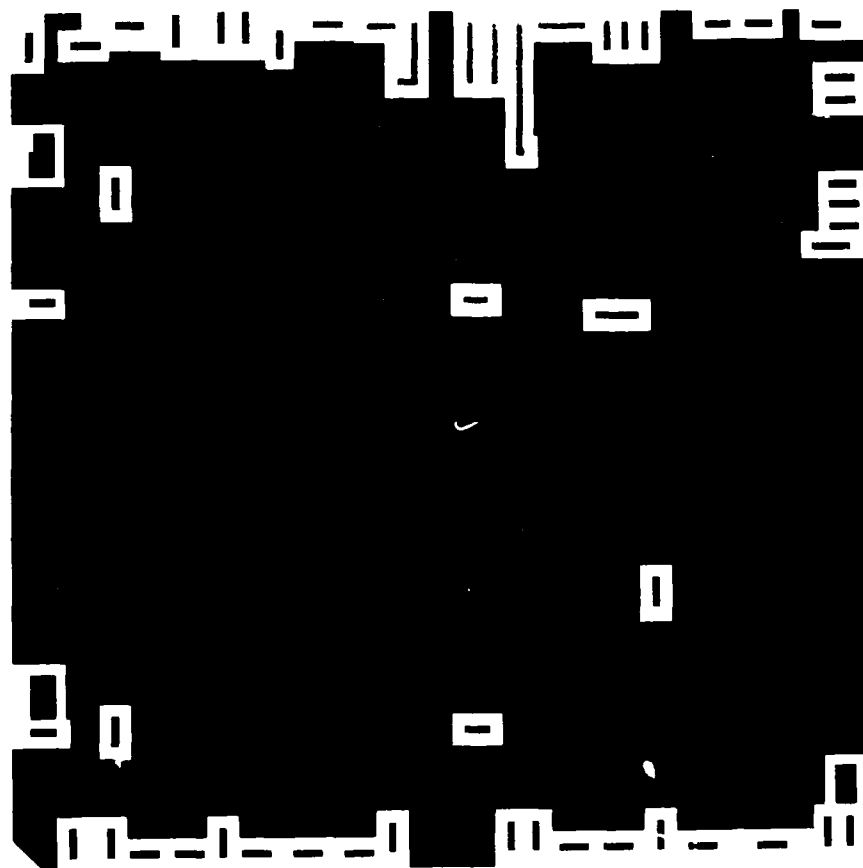
<u>Page</u>	<u>Layer Number</u>	<u>Description</u>
E-2	1	Bond Pads and Vcc Planes
E-3	2	Dielectric
E-4	3	Vdd Plane
E-5	4	Dielectric
E-6	5	Vss Plane
E-7	6	Dielectric
E-8	7	Metal Interconnect
E-9	8	Dielectric
E-10	9	Metal Interconnect
E-11	10	Dielectric
E-12	11	Vss Plane
E-13	12	Dielectric
E-14	13	Metal Interconnect
E-15	14A	Dielectric
E-16	14B	Dielectric
E-17	15	Pads



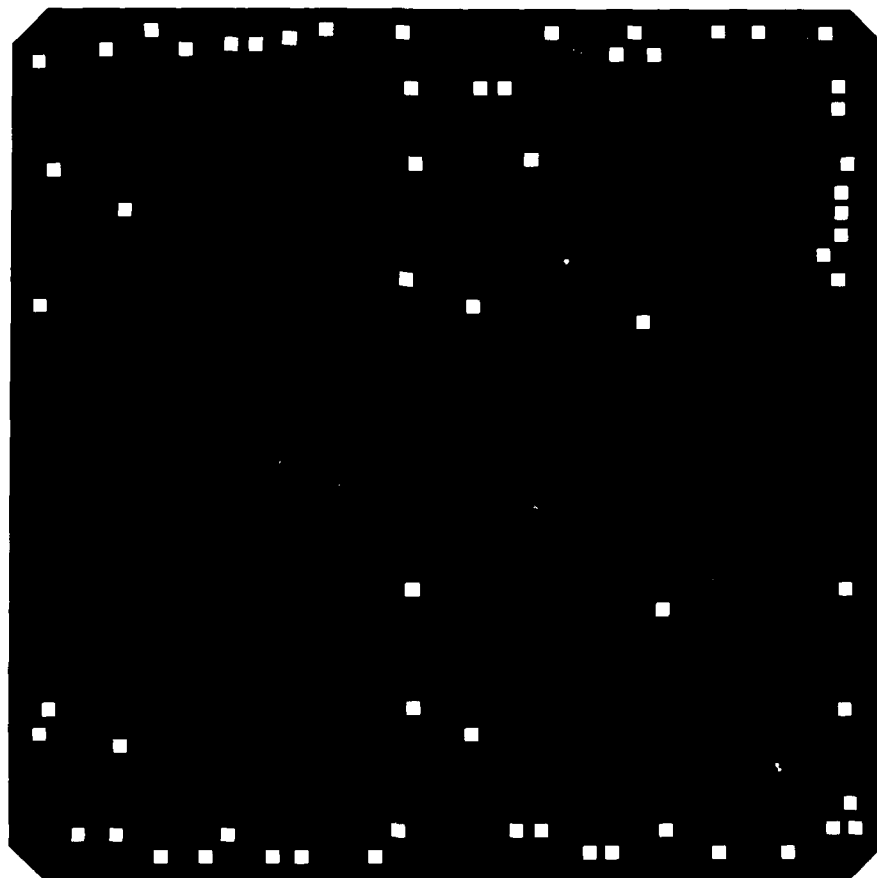
BOND PAD LAYER 1  
VCC PLANE 20X



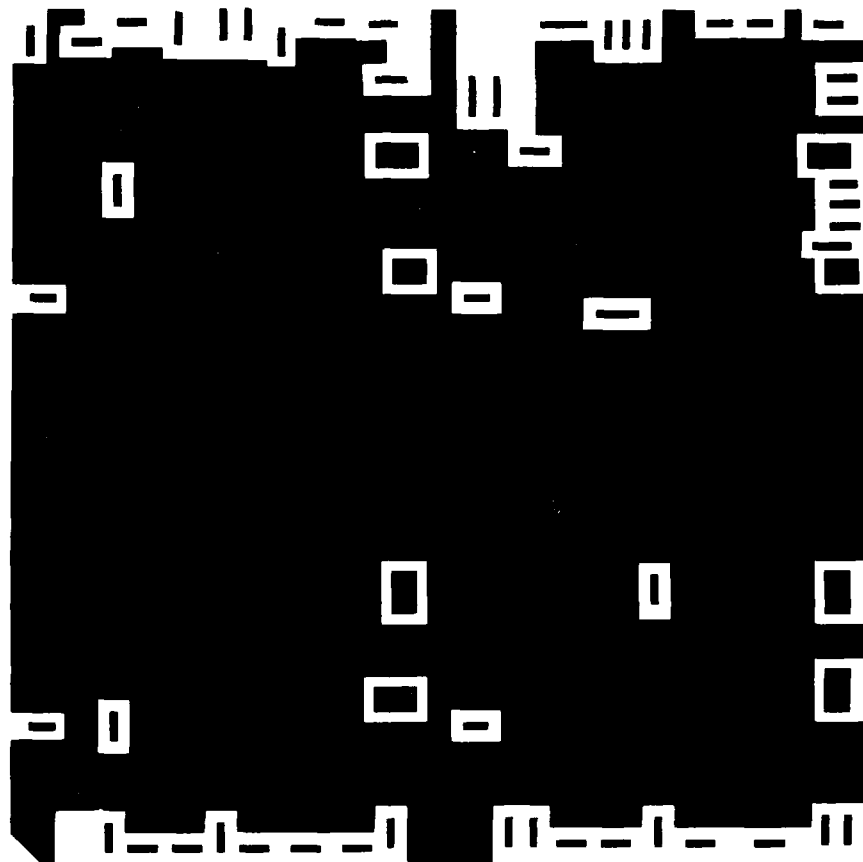
DIELECTRIC LAYER 2



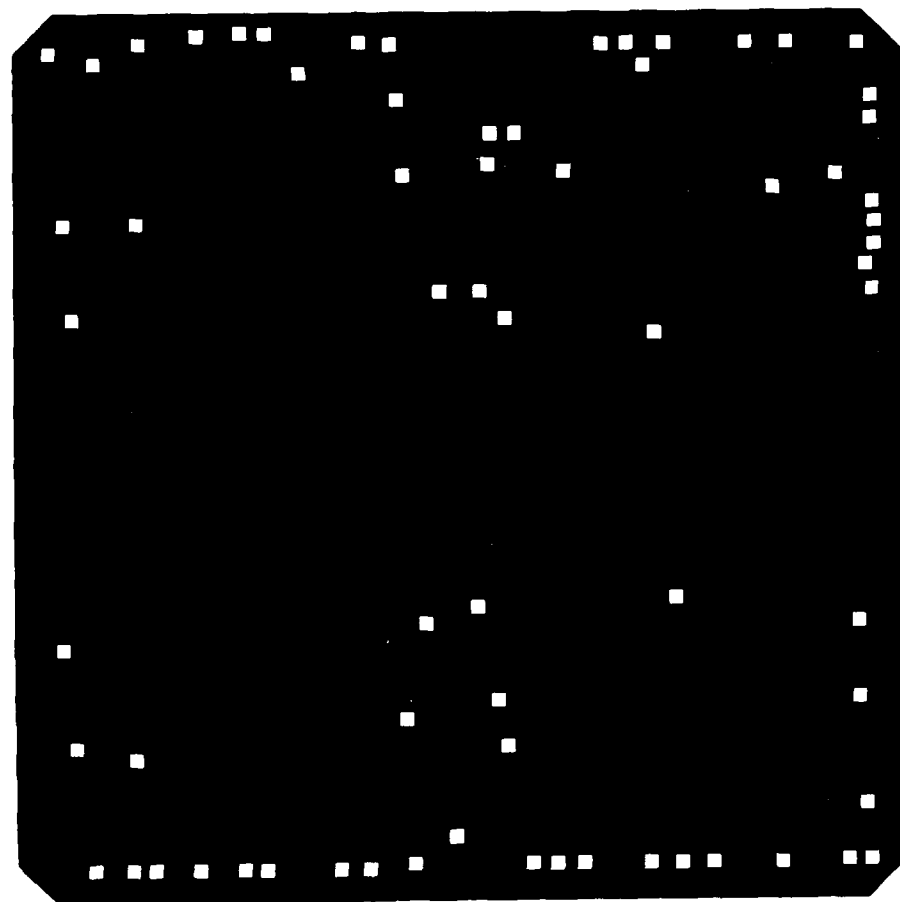
VDD PLANE LAYER 3



DIELECTRIC LAYER 4



VSS PLANE LAYER 5

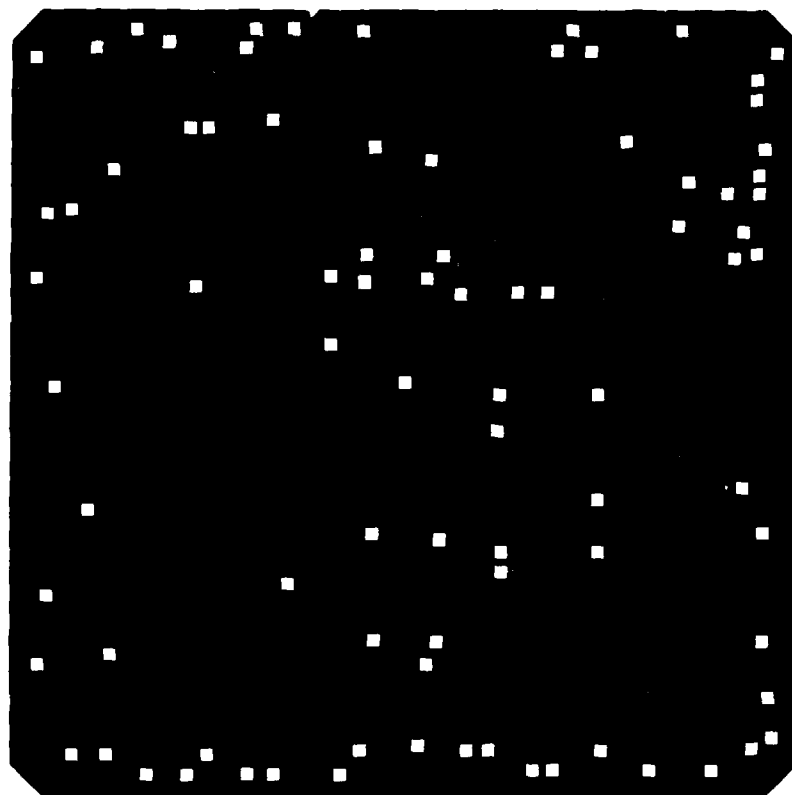


DIELECTRIC LAYER 6

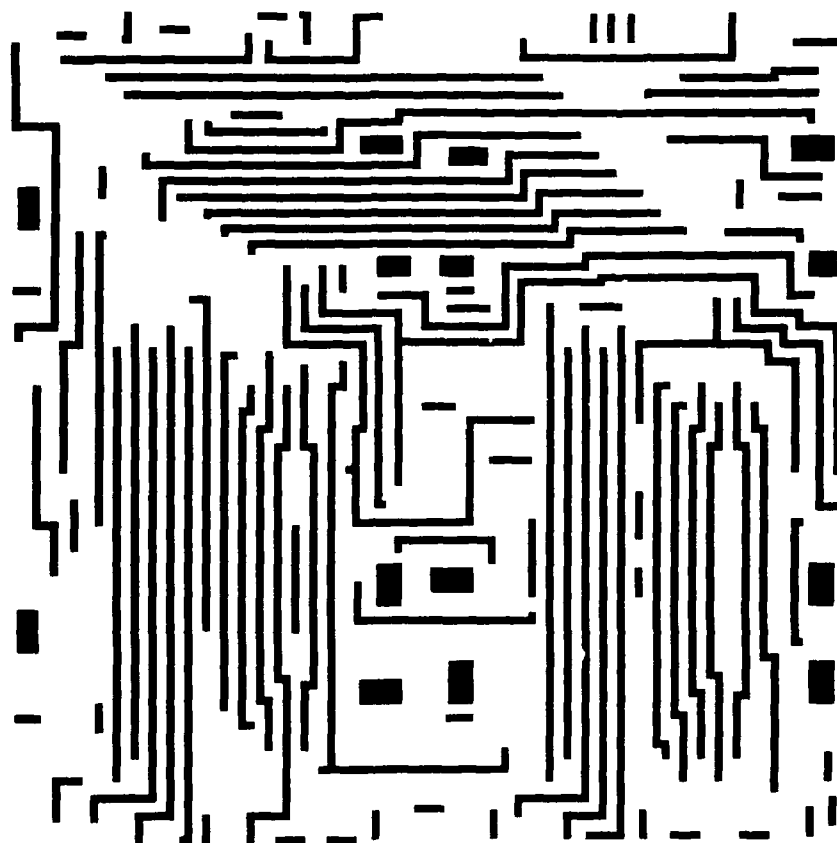




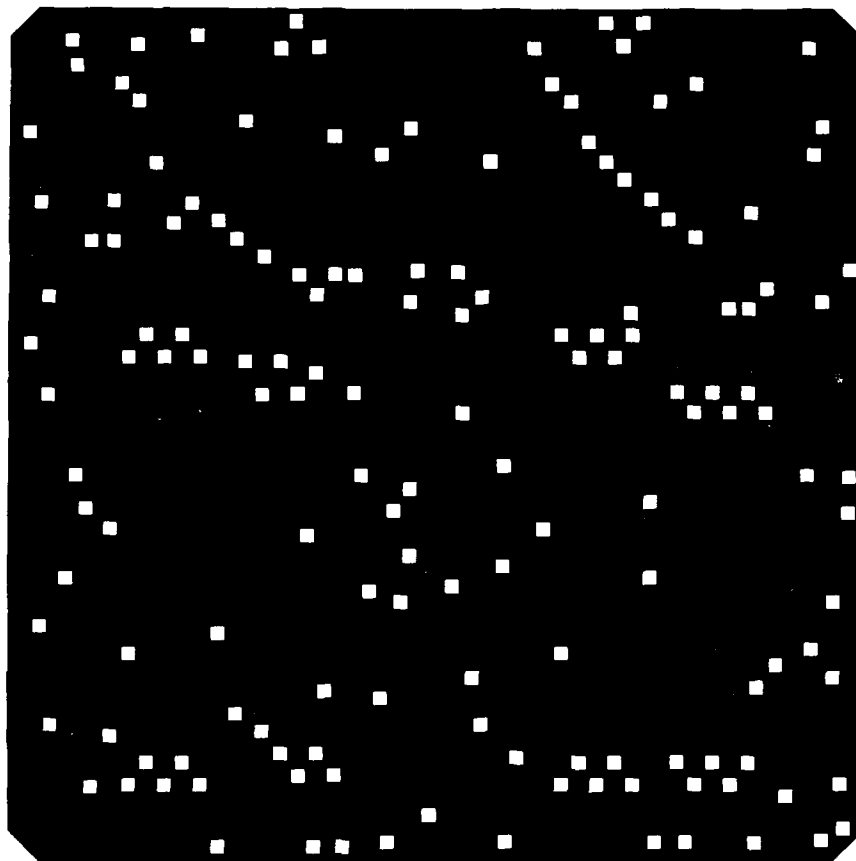
METAL LAYER 7



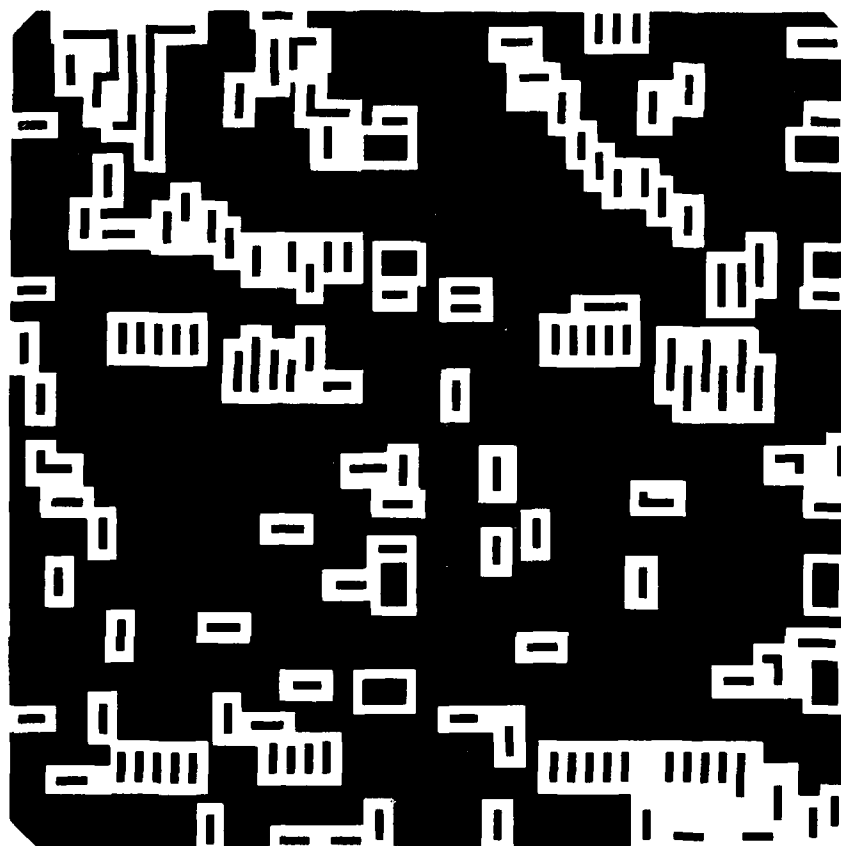
DIELECTRIC LAYER 8



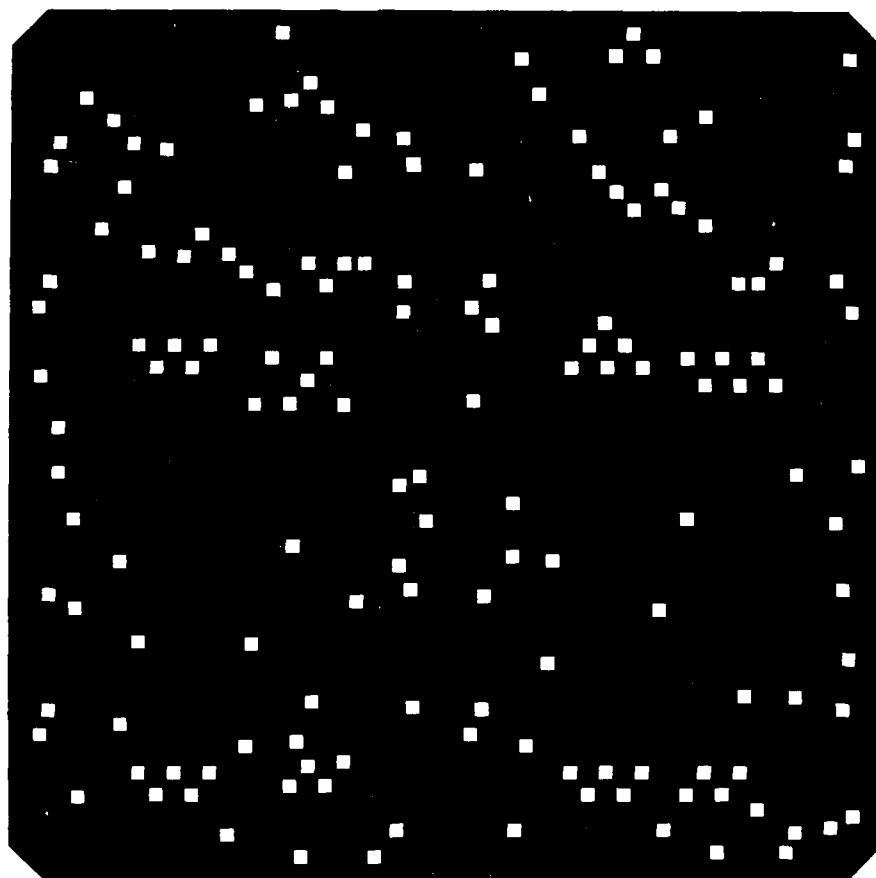
METAL LAYER 9



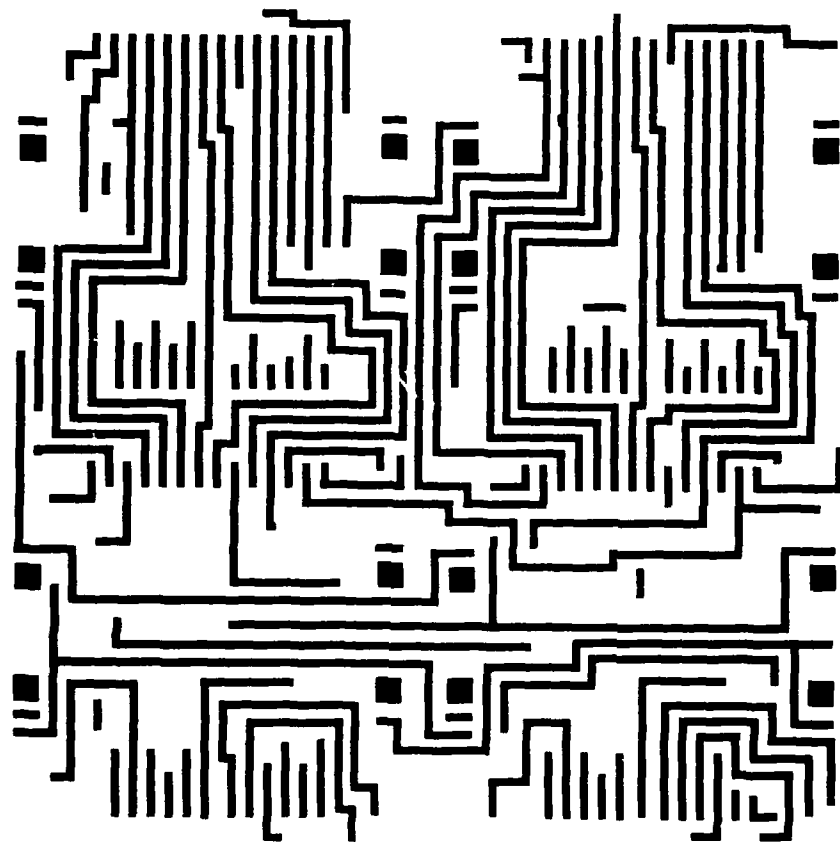
DIELECTRIC LAYER 10



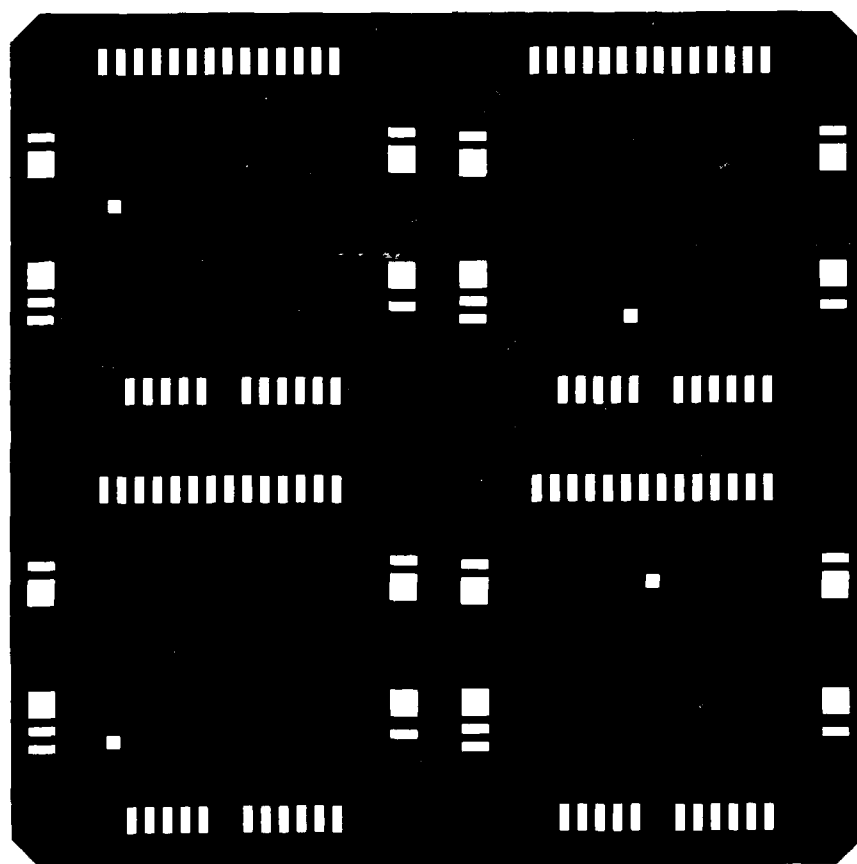
VSS PLANE LAYER 11



DIELECTRIC LAYER 12

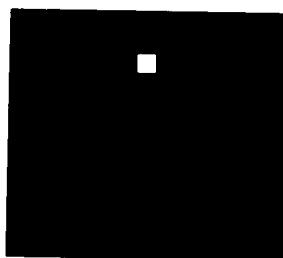
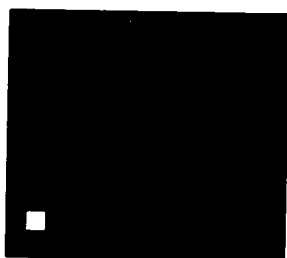
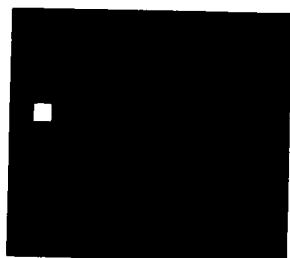


METAL LAYER 13

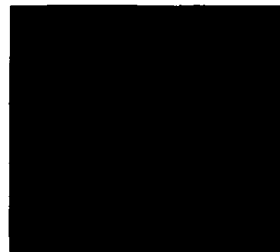


DIELECTRIC LAYER 14A





DIELECTRIC LAYER 14B



PADS LAYER 15

## APPENDIX F

### DETAILED TEST PROCEDURES

This section of the report contains detailed testing procedures used in evaluating the multichip module. Procedures include TAB tape testing, substrate testing, module testing, and RF analysis. All electrical testing was performed on either a Sentry 21, HP8510 Automatic Network Analyzer, or benchtop equipment.

<u>Page</u>	<u>Drawing Number</u>	<u>Document</u>
F-2 - F-5	2437692	Single-chip TAB Test
F-6 - F-9	2437693	X4 Interconnect Module Test
F-10 - F-13	2437694	X4 SRAM Package Test
F-14 - F-18	2437695	Signal Line Test and Modeling Procedure
F-19 - F-24	2437697	Cold Start Power-on Procedure
F-25 - F-30	2437698	Voltage Drop Test Procedure
F-31 - F-36	2437699	Infrared Analysis Procedure
F-37 - F-42	2437700	Maximum Current Delivery Test Procedure

SH 1

[illegible]

## TEST PROCEDURE

### SINGLE CHIP TAB TEST

FOR

LABCOM VHSIC MULTICHIP PROGRAM

[illegible]

71 88217

**F - 2**

EQUIPMENT

- SENTRY 21 TEST SYSTEM
- MODIFIED ELECTROGLAS MODEL 1034X PROBE STATION

DETAILED TESTS

1. Place the DBUP tape for SRAM probe on the tape drive of the Sentry 21. Reset the system. Type in a "2" for the tape function and press <RETURN>. The system will start to copy the tape onto the disk. This will take about ten minutes.
2. Place the performance board in the Sentry test head. Make sure that the pins line up. Pin 1 is at the bottom of the tester. It is marked on the tester and the performance board.

Note: It is easier to connect the four cables to the performance board before it is placed in the test head.

3. Turn the probe station power on. Place the controls in the manual mode. Place the TAB probe card into the probe card holder. Connect the DUT board to the performance board.
4. Place the TAB tape onto the chuck. Move the tape under the probes and align the probes with the test points. Use the z-axis and theta adjustments for fine adjust.
5. Once the magnetic tape has been loaded into the system the screen will read :

READY

```

Enter JOB TEST <RETURN>
Enter DIRECT   <RETURN>
Enter time     <RETURN>
Enter date     <RETURN>
Enter STAT3    <RETURN>
Enter LOAD 'SRAM,H' STAT3 KEEP <RETURN>
Enter MANU     <RETURN>
               <RETURN>
  
```

- 5.1 The screen will prompt you with :

TYPE IN PID 'T' AT THE END OF TEST SN1

```

Enter           <RETURN>
  
```



DWN

DATE

SIZE

FSCM NO

DRAWING NO

REV

A

96214

2437692

ISSUE DATE

SCALE

SHEET

2

5.2 The system will prompt you with :

PRESS AUTO BUTTON ON OPTION D AND HIT RETURN

Enter <RETURN>

6 The system will prompt you with the following questions :

6.1 DOES THIS TEST HEAD HAVE A CLOCK CARD AT PIN 47?

Enter N <RETURN>

6.2 ENTER NOMINAL VDD VALUES :

Enter 3.3 <RETURN>

6.3 ENTER VBB :

Enter -0.5 <RETURN>

6.4 ENTER LOT NO :

Enter 6017 <RETURN>

6.5 ENTER SLICE NO :

Enter 12 <RETURN>

6.6 ENTER FIRST DEVICE S/N :

Enter 1 <RETURN>

6.7 ENTER DEVICE TEMPERATURE :

Enter 25 <RETURN>

6.8 ARE THE OUTPUT LOADS TO BE USED? (Y OR N)

Enter Y <RETURN>

6.9 CHOOSE THE PPM PATTERN DESIRED (0-9)

Enter 7 <RETURN>

Enter POD DOF '601712' <RETURN>  
<RETURN>



OWN DATE

SIZE FSCM NO

A 96214

DRAWING NO  
2437692

REV

ISSUE DATE

SCALE

SHEET 3

7. The SRAM test will begin and will take approximately 1.5 minutes.

When testing is complete, place a new device for test under the probes and align.

Enter PID 'T' <RETURN>

Testing will continue.

8. The system will always generate the error :

OPEN PIN 56

OPEN PIN 57

Disregard this message.

9. When the test is completed, the system will display :

PID

Enter POD

10. To make a printout of the results :

Enter COPY '601712' LP

To copy to a magnetic tape :

Enter COPY '601712' MTR1

11. Upon completion of testing, place the DBUP tape back on the system tape drive.

Enter DBUP VERIFY <RETURN>

This procedure will take approximately 15 minutes. Put the tape back where you found it.



DWN

DATE

SIZE

FSCM NO

DRAWING NO

REV

A

96214

2437692

ISSUE DATE

SCALE

SHEET

4

SH 1

[illegible]

## TEST PROCEDURE

#### X4 INTERCONNECT MODULE TEST

FOR

LABCOM VHSC MULTICHIP PROGRAM

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EQUIPMENT

- SENTRY 21 TEST SYSTEM
- MODIFIED ELECTROGLAS MODEL 1034X PROBE STATION

DETAILED TESTS

1. Place the DBUP tape for SRAM probe on the tape drive of the Sentry 21. Reset the system. Type in a "2" for the tape function and press <RETURN>. The system will start to copy the tape onto the disk. This will take about ten minutes.
2. Place the performance board in the Sentry test head. Make sure that the pins line up. Pin 1 is at the bottom of the tester. It is marked on the tester and the performance board.

Note: It is easier to connect the four cables to the performance board before it is placed in the test head.

3. Turn the probe station power on. Place the controls in the manual mode. Place the X4 INTERCONNECT MODULE probe card into the probe card holder. Connect the DUT board to the performance board.
4. Place the MODULE onto the chuck. Move the tape under the probes and align the probes with the test points. Use the z-axis and theta adjustments for fine adjust.
5. Once the magnetic tape has been loaded into the system the screen will read :

READY

```


Enter JOB TEST <RETURN>
Enter DIRECT   <RETURN>
Enter time     <RETURN>
Enter date     <RETURN>
Enter STAT3    <RETURN>
Enter LOAD 'SRAM,H' STAT3 KEEP <RETURN>
Enter MANU     <RETURN>
               <RETURN>
  
```

- 5.1 Using the SRAM selector switch, choose the first SRAM.

The screen will prompt you with :

TYPE IN PID 'T' AT THE END OF TEST SN1

Enter                   <RETURN>

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5.2 The system will prompt you with :

PRESS AUTO BUTTON ON OPTION D AND HIT RETURN

Enter <RETURN>

6 The system will prompt you with the following questions :

6.1 DOES THIS TEST HEAD HAVE A CLOCK CARD AT PIN 47?

Enter N <RETURN>

6.2 ENTER NOMINAL VDD VALUES :

Enter 3.3 <RETURN>

6.3 ENTER VBB :

Enter -0.5 <RETURN>

6.4 ENTER LOT NO :

Enter 6017 <RETURN>

6.5 ENTER SLICE NO :

Enter 12 <RETURN>

6.6 ENTER FIRST DEVICE S/N :

Enter 1 <RETURN>

6.7 ENTER DEVICE TEMPERATURE :

Enter 25' <RETURN>

6.8 ARE THE OUTPUT LOADS TO BE USED? (Y OR N)

Enter Y <RETURN>

6.9 CHOOSE THE PPM PATTERN DESIRED (0-9)

Enter 7 <RETURN>

Enter POD DOF '601712' <RETURN>  
<RETURN>



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7. The SRAM test will begin and will take approximately 1.5 minutes.

When testing is complete, change the SRAM selector switch to the next position. Repeat until all four SRAMs are tested.

Enter PID 'T' <RETURN>

Testing will continue.

8. The system will always generate the error :

OPEN PIN 56

OPEN PIN 57

Disregard this message.

9. When the test is completed, the system will display :

PID

Enter POD

10. To make a printout of the results :

Enter COPY '601712' LP


To copy to a magnetic tape :

Enter COPY '601712' MTR1

11. Upon completion of testing, place the DBUP tape back on the system tape drive.

Enter DBUP VERIFY <RETURN>

This procedure will take approximately 15 minutes. Put the tape back where you found it.

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EQUIPMENT

- SENTRY 21 TEST SYSTEM

DETAILED TESTS

1. Place the DBUP tape for SRAM probe on the tape drive of the Sentry 21. Reset the system. Type in a "2" for the tape function and press <RETURN>. The system will start to copy the tape onto the disk. This will take about ten minutes.
2. Place the performance board in the Sentry test head. Make sure that the pins line up. Pin 1 is at the bottom of the tester. It is marked on the tester and the performance board.

Note: It is easier to connect the four cables to the performance board before it is placed in the test head.

3. Connect the DUT board to the performance board.
4. Place the PACKAGE into the test socket.
5. Once the magnetic tape has been loaded into the system the screen will read :

READY


Enter JOB TEST <RETURN>  
Enter DIRECT <RETURN>  
Enter time <RETURN>  
Enter date <RETURN>  
Enter STAT3 <RETURN>  
Enter LOAD 'SRAM,H' STAT3 KEEP <RETURN>  
Enter MANU <RETURN>

- 5.1 Using the SRAM selector switch, choose the first SRAM.

The screen will prompt you with :

TYPE IN PID 'T' AT THE END OF TEST SN1

Enter <RETURN>

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5.2 The system will prompt you with :

PRESS AUTO BUTTON ON OPTION D AND HIT RETURN

Enter <RETURN>

6 The system will prompt you with the following questions :

6.1 DOES THIS TEST HEAD HAVE A CLOCK CARD AT PIN 47?

Enter N <RETURN>

6.2 ENTER NOMINAL VDD VALUES :

Enter 3.3 <RETURN>

6.3 ENTER VBB :

Enter -0.5 <RETURN>

6.4 ENTER LOT NO :

Enter 6017 <RETURN>

6.5 ENTER SLICE NO :

Enter 12 <RETURN>

6.6 ENTER FIRST DEVICE S/N :

Enter 1 <RETURN>

6.7 ENTER DEVICE TEMPERATURE :

Enter 25 <RETURN>


6.8 ARE THE OUTPUT LOADS TO BE USED? (Y OR N)

Enter Y <RETURN>

6.9 CHOOSE THE PPM PATTERN DESIRED (0-9)

Enter 7 <RETURN>

Enter POD DOF '601712' <RETURN>  
<RETURN>

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7. The SRAM test will begin and will take approximately 1.5 minutes.

When testing is complete, change the SRAM selector switch to the next position. Repeat until all four SRAMs are tested.

Enter PID 'T' <RETURN>

Testing will continue.

8. The system will always generate the error :

OPEN PIN 56

OPEN PIN 57

Disregard this message.

9. When the test is completed, the system will display :

PID

Enter POD

10. To make a printout of the results :

Enter COPY '601712' LP

To copy to a magnetic tape :

Enter COPY '601712' MTR1

11. Upon completion of testing, place the DBUP tape back on the system tape drive.

Enter DBUP VERIFY <RETURN>

This procedure will take approximately 15 minutes. Put the tape back where you found it.



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SH 1


LABCOM VHSIC MULTICHIP PROGRAM

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C



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## I. SIGNAL LINE - RESISTANCE MEASUREMENT

- A. This test will measure the resistance between the outside package lead to the inside pad of a given signal line.
1. The 196-lead package has 22 unique signal lines that differ in line length due to the fan-out effect required to distribute the signal line through the package wall to the outside package lead.
  2. Although the resistance will be small, there will be a measurable difference in the resistance of signal lines of different length. Resistance measurements will be a check for metalization problems or other gross problems which may exist inside the package wall.
  3. The 308-lead package has 35 unique signal lines each having a measurable difference in resistance.
- B. The resistance measurements will require an ohmmeter with fine-tip probes or a probe station.
1. The resulting data will be graphs and tables of lead resistance versus location in the package or versus lead length.

## II. TOUCHSTONE - DISTRIBUTED ELEMENT - MODEL

- A. The TOUCHSTONE distributed element model is a computer model that exhibits electrical characteristics similar to those of the actual LABCOM package.
1. Distributed element means the computer will model the package by interconnecting microstrip, stripline, ribbons, and other "distributed" elements instead of using R, L, and C discrete elements.
  2. Based on actual package metalization and dielectric construction, a model will be generated that describes the package in terms of an interconnection of TOUCHSTONE-distributed element commands.
- B. The TOUCHSTONE modeling requires an HP9836 computer with sufficient memory and -- of course the TOUCHSTONE software.
1. The TOUCHSTONE model will result in a graph and/or table of full 2-port S-parameters versus frequency. S11 is return loss (fwd), S21 is transmission loss (fwd), S12 is transmission loss (rvrs), S22 is return loss (rvrs). Each parameter will be plotted in dB versus frequency.


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### III. TEST FIXTURE FABRICATION

- A. The test fixture must be compatible with the HP8510 network analyzer which will be used to perform most of the tests. The test fixture will allow actual measurements to be made of the 196- and 308-lead LBCOM package signal lines.
1. The test fixture will consist of 50 ohm transmission line connected to the package outside leads and will serve as a means of injecting test signals into the package. Inside each package under test there will be 50 ohm transmission lines epoxied to the package base, one end of which will be bonded to a signal line pad on the inside bond pad shelf of the package, and the other end bonded to the corresponding pad on the opposite side of the package. The inner 50 ohm transmission line will serve to pass the test signals from the HP8510 network analyzer and/or other test equipment completely through the package - this will allow measurement of the transmission characteristics of the package.
  2. Transmission lines will also be mounted in such a way that the adjacent lead coupling can be measured.

### IV. (100 MHz) CLOCK SIGNAL AND RISE TIME SENSITIVITY TEST.

- A. Measure the distortion of a typical 100 MHz clock signal that is caused by the package signal line network.
1. Apply a 100 MHz clock signal into a 0 degree power splitter. Connect one clock signal line directly to an oscilloscope input amplifier. Connect the other clock signal line to the package and connect the signal line after passing through the package to another input channel of the oscilloscope. Use the trigger output of the clock signal generator to trigger the oscilloscope. The display on the oscilloscope will display two traces, one trace will be the undistorted clock signal and the other display will be the resulting signal after passing through the package. A direct comparison of the distortion caused by the package can be made.
  2. The frequency of the clock signal can be varied to determine any sensitivity the package may have to frequency. The rise time can also be adjusted to measure the sensitivity of the package to rise time.
- B. The clock signal tests will require a time synthesizer or equivalent signal generator (capable of generating rise times below 1 nano-second), a 1 GHz oscilloscope, a power splitter, and the test fixture.
1. The results will be photographs of clock signals with and without the effects of the package signal lines and will demonstrate any distortion/differences caused by the package.

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## V. HP8510 AUTOMATIC NETWORK ANALYZER MEASUREMENTS


- A. Measure the full 2-port S-parameters of the package signal lines using the HP8510 ANA. The data will include: S11 - Return loss (fwd), S21 - Transmission loss (fwd), S12 - Transmission loss (rev), S22 - Return loss (rev).
  1. Custom software will be used to control the HP8510 to obtain the error-corrected data. The software will allow the test operator to calibrate the ANA over any contiguous frequency range between 45 MHz and 26.8 GHz.
  2. The ANA data will define a full 2-port characterization of the signal lines for the 196-lead and the 308-lead packages. The data will be compared with the TOUCHSTONE model data. The model will be adjusted (if necessary) to agree with the measured data. The measured and modeled data will be compared for each of the unique signal line cases that result from metalization and dielectric construction inside the packages.
- B. The ANA measurements will require an HP8510 ANA, a series 200 or 300 HP computer, control software and support hardware such as: printer, test cables, connectors, test fixture, etc. The test fixture, as described in paragraph III, will use SMA type connectors to interface with the HP8510 ANA test cables.
  1. The results of the ANA test will provide actual package measurement data in the form of tables and graphs. The TOUCHSTONE model will be improved by requiring that it agree with the measured data.

## VI. THE R-L-C LABCOM PACKAGE CHARACTERIZATION - MODEL

- A. Model transformation
  1. The distributed element model as described in paragraph II will be converted to an equivalent R L-C model on TOUCHSTONE. The final "distributed" element values as determined by optimizing the model to the measured data will be converted to R-L-C values. The resulting R-L-C network will be optimized as required to agree with the measured data.

## VII. SUMMARY AND CONCLUSIONS

- A. A final report will be generated to summarize the model, measurements and data.
  1. The report will include graphs, tables, photos, etc. that represent the measured and modeled data. Final conclusions will be made that will summarize the overall performance of the package.

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LABCOM-VMC 196-PIN PACKAGE CHARACTERIZATION TEST  
COLD START POWER-ON TEST PROCEDURE

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Procedure Revision Letter Requirements	3.2
Visual Inspection	3.3
DETAILED TESTS	4.
Setup	4.1
Primary Power Plane	4.2
Secondary Power Plane	4.3
Tertiary Power Plane	4.4

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## 2. LIST OF TEST EQUIPMENT

2.1 Verify that the test equipment is currently certified per Texas Instruments Quality System Procedure 6-2-0. (Stamp).

Equipment	Manufacturer	Part No. (or Model No. Etc)
Function Generator	Hewlett-Packard	3314A
Oscilloscope	Tektronix	2465

## 3. TEST PROCEDURES

3.1 Data will be taken in the form of oscilloscope photographs; a data sheet will not be necessary.

3.2 Observe the latest revision letter to this procedure at the time of the test. (Record).

## 3.3 Visual Inspection

3.3.1 Inspect the unit under test to assure that it is not damaged.

## 4. DETAILED TESTS

## 4.1 Setup

4.1.1 For this test, use an unaltered package (Figure 1).


4.1.2 With the function generator turned off, solder the positive lead from the function generator to the primary power plane pins (25, 74, 123, 172) and the return lead to the ground pins (9, 41, 58, 90, 107, 139, 156, 188). See Figure 2.

## 4.2 Primary Power Plane

4.2.1 With the oscilloscope, probe a point on the primary power plane relative to the ground plane.

4.2.2 Pulse the power plane with the function generator. Observe and photograph the power-up wave form.

4.2.3 Remove the power leads one at a time, repeating paragraph 4.2.2 after removing each one.

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4.3 Secondary Power Plane

4.3.1 Solder the positive lead from the function generator to the secondary power plane pins (17, 66, 115, 164) and repeat paragraph 4.2 for the secondary plane.

4.4 Tertiary Power Plane

Solder the positive lead from the function generator to the tertiary power plane pins (33, 82, 131, 180) and repeat paragraph 4.2 for the tertiary plane.

5. FIGURES

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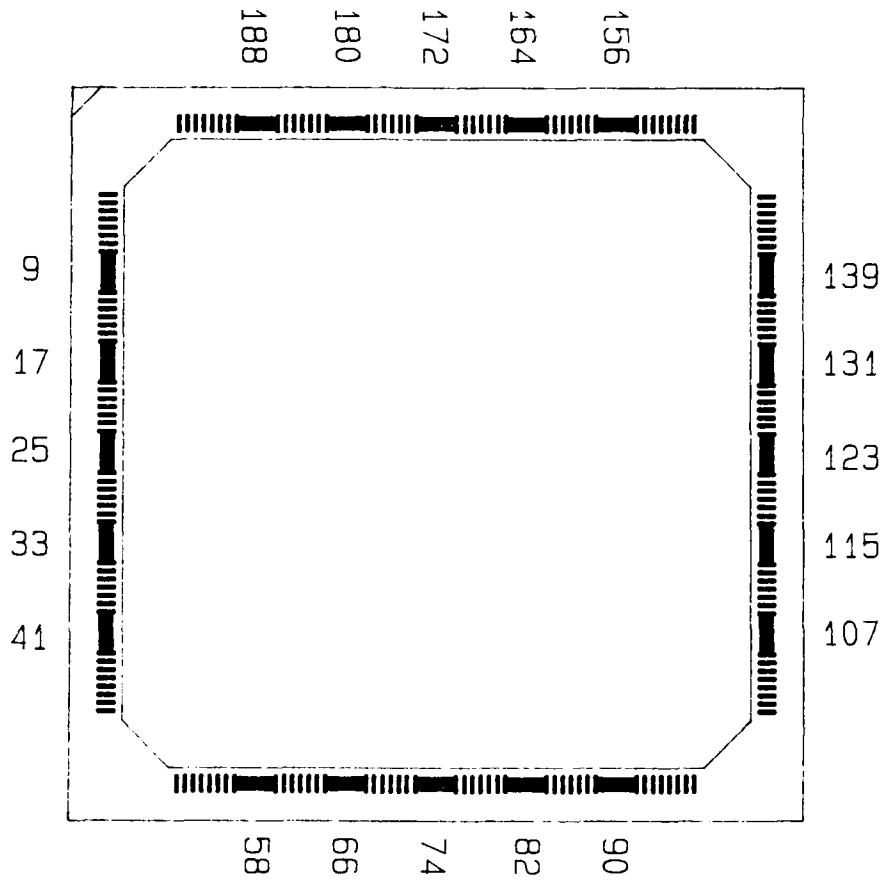



Figure 1.

 <b>TEXAS</b> <b>INSTRUMENTS</b> <small>Dallas, Texas</small>	DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
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# LABCOM 196-PIN PACKAGE

## POWER-UP TEST

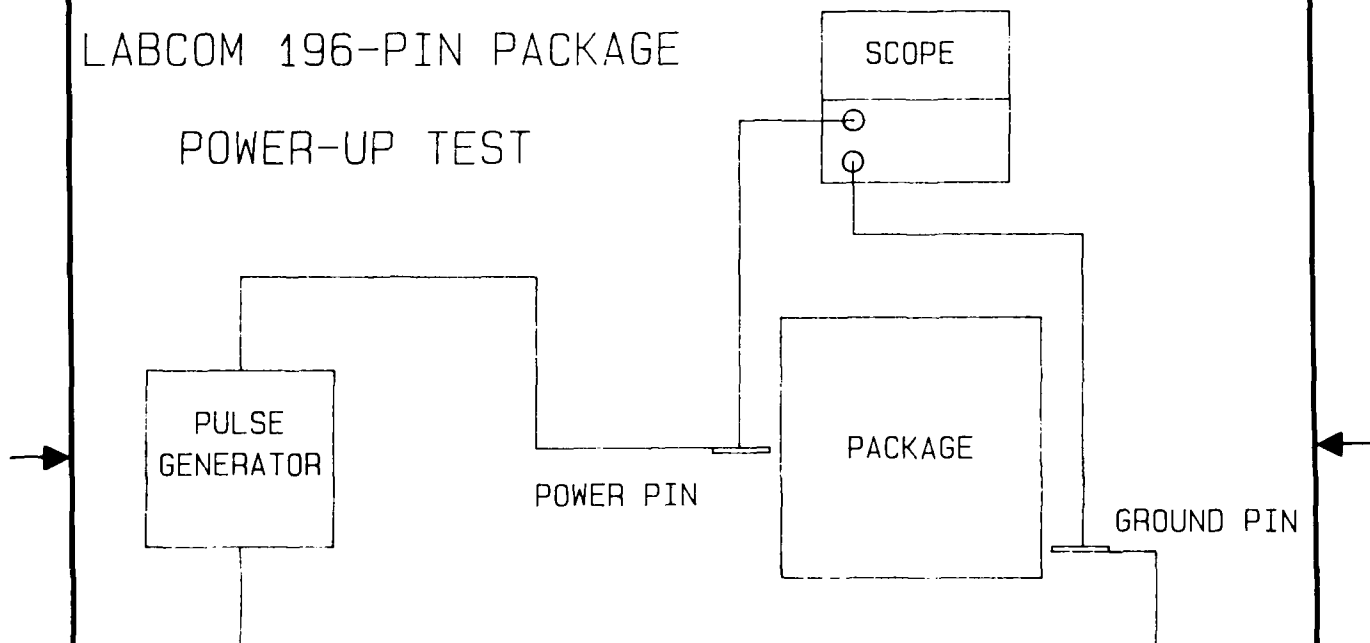


Figure 2.

 <b>TEXAS</b> <b>INSTRUMENTS</b> <small>Dallas, Texas</small>	OWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
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## LABCOM-VMC 196-PIN PACKAGE CHARACTERIZATION TEST

### VOLTAGE DROP TEST PROCEDURE

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## 1. TABLE OF TESTS

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## 2. LIST OF TEST EQUIPMENT

2.1 Verify that the test equipment is currently certified per Texas Instruments Quality System Procedure 6-2-0. (Stamp).

Equipment	Manufacturer	Part No. (or Model No. Etc)
-----	-----	-----
DC Power Supply	Hewlett-Packard	6033A
Digital Multimeter	Hewlett-Packard	3478A
Switch Network	Texas Instruments	N/A

## 3. TEST PROCEDURES

3.1 Data will be recorded in the procedure. Data Sheet is not necessary.

3.2 Observe the latest revision letter to this procedure at the time of the tests. (Record).

## 3.3 Visual Inspection

3.3.1 Inspect the unit under test to assure that it is not damaged.

## 4. DETAILED TESTS

## 4.1 Setup

4.1.1 For this test, use a package that has the power and ground bond pads wired to the floor of the package. (Figure 1).

4.1.2 With all switches set to OFF, connect the power and return leads from the switch box to the poles of the power supply.

4.1.3 Solder each of the distribution wires of the switch box to the appropriate power and ground pins of the package. (Figure 2).

4.1.4 Use a digital multimeter to measure the current flowing in each test.

## 4.2 Primary Power Plane

## CAUTION!

Use the current limiting feature of the power supply to prevent damage to the package.



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- 4.2.1 Using the switch network, connect the primary power plane pins (switches 25, 74, 123, and 172) to POWER and GROUND in various combinations to allow current to flow through the plane.
- 4.2.2 Use the digital multimeter to measure and record the current and voltage drops across the various parts of the plane.
- 4.2.3 Set power pin switches 25, 74, 123, and 172 to POWER and ground pin switches 9, 41, 58, 90, 107, 139, 156, and 188 to GROUND. Measure the current and voltage drops from the end of the power pins to the bond pads and record the data.
- 4.3 Secondary Power Plane
- 4.3.1 Repeat paragraph 4.2 for the secondary power plane using switches 17, 66, 115, and 164.
- 4.4 Tertiary Power Plane
- 4.4.1 Repeat paragraph 4.2 for the tertiary power plane using switches 33, 82, 131, and 180.
- 4.5 Ground Plane
- 4.5.1 Perform paragraphs 4.2.1 and 4.2.2 on the ground plane. Ground plane pins are wired to switches 9, 41, 58, 90, 107, 139, 156, and 188.
- 4.5.2 Set switches 17, 25, 33, 66, 74, 82, 115, 123, 131, 164, 172, and 180 to POWER and switches 9, 41, 58, 90, 107, 139, 156, and 188 to GROUND. Measure and record the current and voltage drops from the end of the ground pins to the bond pad.
5. FIGURES



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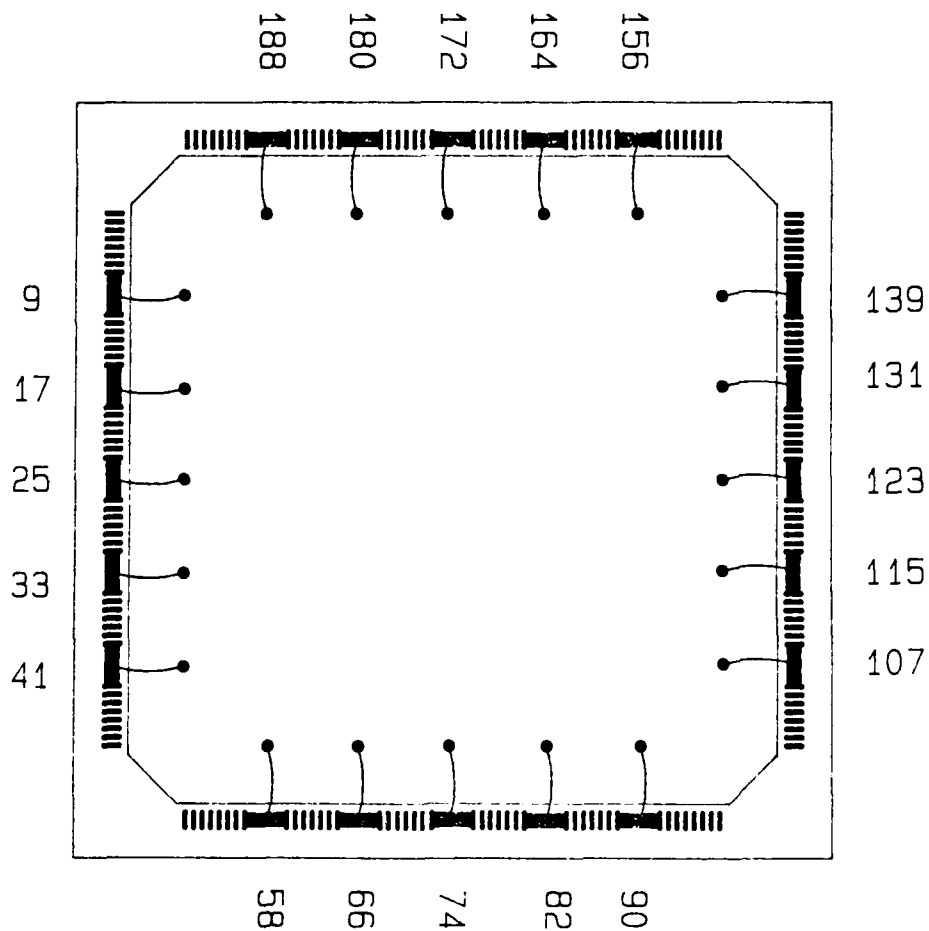



Figure 1.

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LABCOM 196-PIN PACKAGE  
LOW CURRENT VOLTAGE DROP TEST

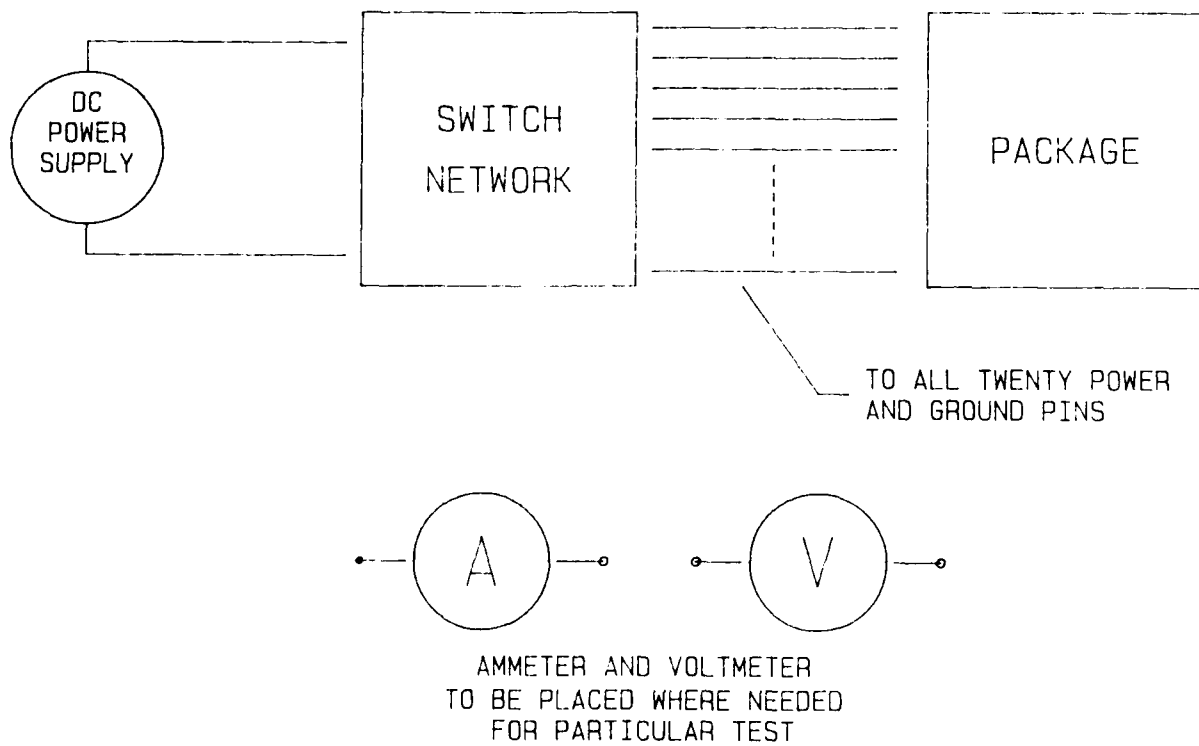



Figure 2.

 <b>TEXAS</b> <b>INSTRUMENTS</b> <small>Dallas, Texas</small>	DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
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LABCOM-VMC 196-PIN PACKAGE CHARACTERIZATION TEST  
INFRARED ANALYSIS TEST PROCEDURE

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## 1. TABLE OF TESTS

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Primary Power Plane	4.2
Secondary Power Plane	4.3
Tertiary Power Plane	4.4
Ground Plane	4.5

## 2. LIST OF TEST EQUIPMENT

2.1 Verify that the test equipment is currently certified per Texas Instruments Quality System Procedure 6-2-0. (Stamp).

2.2 Equipment	Manufacturer	Part No. (or Model No. Etc)
-----	-----	-----
DC Power Supply	Hewlett-Packard	6033A
Digital Multimeter	Hewlett-Packard	3478A
Color Thermograph	UTi	9000
Switch Network	Texas Instruments	N/A

## 3. TEST PROCEDURES

3.1 Data will be recorded in the procedure. Data Sheet is not necessary.

3.2 Observe the latest revision letter to this procedure at the time of the tests. (Record).

## 3.3 Visual Inspection

3.3.1 Inspect the unit under test to assure that it is not damaged.

## 4. DETAILED TESTS

## 4.1 Setup

4.1.1 For this test, use a package that has the power and ground bond pads wired to the floor of the package. (Figure 1). The package will be painted flat black.

4.1.2 With all switches set to OFF, connect the power and return leads from the switch box to the poles of the power supply.

4.1.3 Solder each of the distribution wires of the switch box to the appropriate power and ground pins of the package. (Figure 2).

4.1.4 Use a digital multimeter to measure the current flowing in each test.

4.1.5 Place the package in front of the color thermograph sensor and set up the thermograph to analyze hot spots in the package.



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## 4.2 Primary Power Plane

**CAUTION!**

Use the current limiting feature of the power supply to prevent damage to the package.

4.2.1 Using the switch network, connect the primary power plane pins (switches 25, 74, 123, and 172) to POWER and GROUND in various combinations to allow current to flow through the plane.

4.2.2 Use the digital multimeter to measure and record the current. Monitor the temperature of the package structures (vias, leads, etc.) and record the temperatures versus the current. Photograph the thermograph display at key current levels.

4.2.3 Set power pin switches 25, 74, 123, and 172 to POWER and ground pin switches 9, 41, 58, 90, 107, 139, 156, and 188 to GROUND. Measure the current and temperature of the package structures and photograph the display at key current levels.

## 4.3 Secondary Power Plane

4.3.1 Repeat paragraph 4.2 for the secondary power plane using switches 17, 66, 115, and 164.

## 4.4 Tertiary Power Plane


4.4.1 Repeat paragraph 4.2 for the tertiary power plane using switches 33, 82, 131, and 180.

## 4.5 Ground Plane

4.5.1 Perform paragraphs 4.2.1 and 4.2.2 on the ground plane. Ground plane pins are wired to switches 9, 41, 58, 90, 107, 139, 156, and 188.

4.5.2 Set switches 17, 25, 33, 66, 74, 82, 115, 123, 131, 164, 172, and 180 to POWER and switches 9, 41, 58, 90, 107, 139, 156, and 188 to GROUND. Measure and record the current and temperature of the package structures and photograph the display at key current levels.

## 5. FIGURES

 <b>TEXAS</b> <b>INSTRUMENTS</b> <small>Dallas Texas</small>	OWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
			<b>A</b>	<b>96214</b>	2437699	
ISSUE DATE			SCALE		SHEET 4	

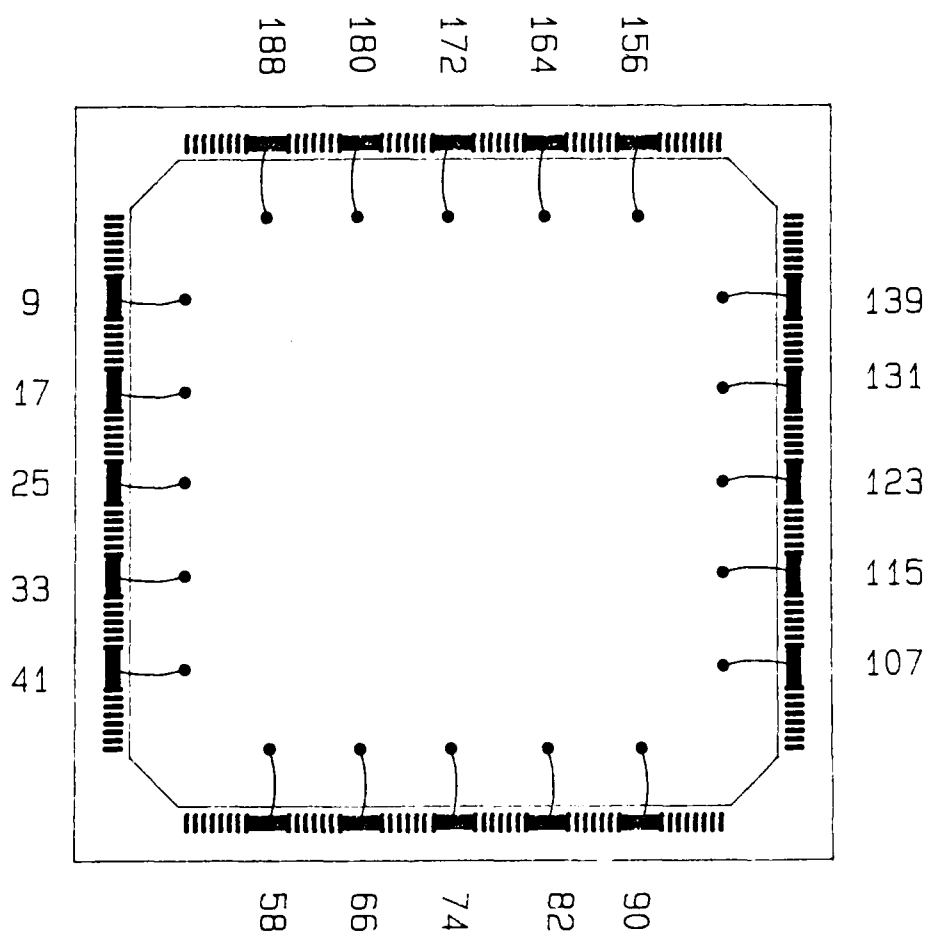



Figure 1.

 <b>TEXAS INSTRUMENTS</b> <small>Dallas, Texas</small>	DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		A	96 214	2437699	
SCALE			SHEET		5	

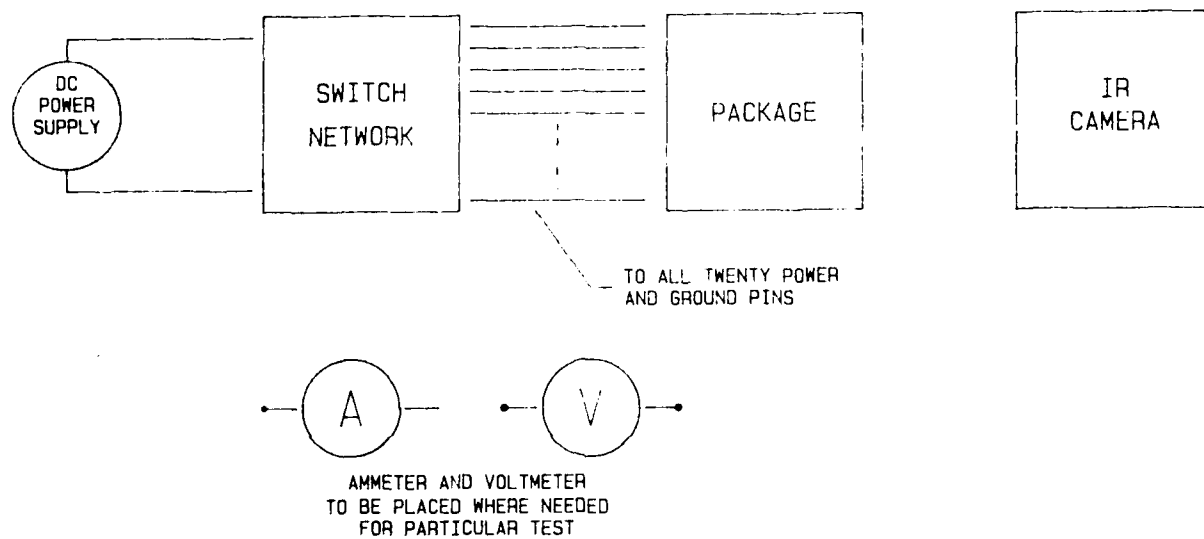
LABCOM 196-PIN PACKAGE  
HIGH CURRENT THERMAL TEST

Figure 2.

**TEXAS**  
**INSTRUMENTS**  
Dallas, Texas

DWN

DATE

SIZE

FSCM NO

DRAWING NO

REV

**A****96214**

2437699

ISSUE DATE

SCALE

SHEET

6

SH 1

LABCOM-VMC 196-PIN PACKAGE CHARACTERIZATION TEST

MAXIMUM CURRENT DELIVERY, DESTRUCTIVE TEST PROCEDURE

A  
B  
C

71 88335


**F - 37**

TABLE OF CONTENTS

Paragraph No.	Title	Sheet No.
1.	TABLE OF TESTS	2
2.	LIST OF TEST EQUIPMENT	3
3.	TEST PROCEDURES	3
4.	DETAILED TESTS	3
5.	FIGURES	4

1. TABLE OF TESTS

Name	Paragraph No.
Documentation Requirements	3.1
Procedure Revision Letter Requirements	3.2
Visual Inspection	3.3
DETAILED TESTS	4.
Setup	4.1
Primary Power Plane	4.2
Secondary Power Plane	4.3
Tertiary Power Plane	4.4
Ground Plane	4.5

	DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		A	96214	2437700	
			SCALE		SHEET	2



## 2. LIST OF TEST EQUIPMENT

2.1 Verify that the test equipment is currently certified per Texas Instruments Quality System Procedure 6-2-0. (Stamp).

2.2 Equipment	Manufacturer	Part No. (or Model No. Etc)
-----	-----	-----
DC Power Supply	Hewlett-Packard	6033A
Digital Multimeter	Hewlett-Packard	3478A
Color Thermograph	UTi	9000
Switch Network	Texas Instruments	N/A

## 3. TEST PROCEDURES

3.1 Data will be recorded in the procedure. Data Sheet is not necessary.

3.2 Observe the latest revision letter to this procedure at the time of the tests. (Record).

3.3 Visual Inspection

3.3.1 Inspect the unit under test to assure that it is not damaged.

## 4. DETAILED TESTS

4.1 Setup

4.1.1 For this test, use a package that has the power and ground bond pads wired to the floor of the package. (Figure 1). The package will be painted flat black.

4.1.2 With all switches set to OFF, connect the power and return leads from the switch box to the poles of the power supply.

4.1.3 Solder each of the distribution wires of the switch box to the appropriate power and ground pins of the package. (Figure 2).

4.1.4 Use a digital multimeter to measure the current flowing in each test.

4.1.5 Place the package in front of the color thermograph sensor and set up the thermograph to analyze hot spots in the package.



DWN

DATE

SIZE

FSCM NO

A

96214

DRAWING NO

2437700

REV

ISSUE DATE

SCALE

SHEET

3

## 4.2 Primary Power Plane

**CAUTION!**

Use the current limiting feature of the power supply to prevent damage to the package until you are ready to destroy the planes.

4.2.1 Using the switch network, connect the primary power plane pins (switches 25, 74, 123, and 172) to POWER and GROUND in various combinations to allow current to flow through the plane.

4.2.2 Use the digital multimeter to measure and record the current. Monitor the temperature of the package structures (vias, leads, etc.). Continue to increase the current until the power plane is destroyed. Record the current at which destruction occurs. Photograph the thermograph display at key current levels.

## 4.3 Secondary Power Plane

4.3.1 Repeat paragraph 4.2 for the secondary power plane using switches 17, 66, 115, and 164.

## 4.4 Tertiary Power Plane

4.4.1 Repeat paragraph 4.2 for the tertiary power plane using switches 33, 82, 131, and 180.


## 4.5 Ground Plane

4.5.1 Repeat paragraph 4.2 on the ground plane. Ground plane pins are wired to switches 9, 41, 58, 90, 107, 139, 156, and 188.

4.5.2 For the next test, a new package (see paragraph 4.1.1) will be needed.

4.5.3 Set switches 17, 25, 33, 66, 74, 82, 115, 123, 131, 164, 172, and 180 to POWER and switches 9, 41, 58, 90, 107, 139, 156, and 188 to GROUND. Measure and record the current and temperature of the package structures and photograph the display at key current levels. Continue to increase the current until some structure of the package is destroyed. Record the current at which destruction occurs.

## 5. FIGURES

 <b>TEXAS INSTRUMENTS</b> <small>Dallas, Texas</small>	OWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		A	96214	2437700	
			SCALE		SHEET	4

DWG NO 2437700

SH 5

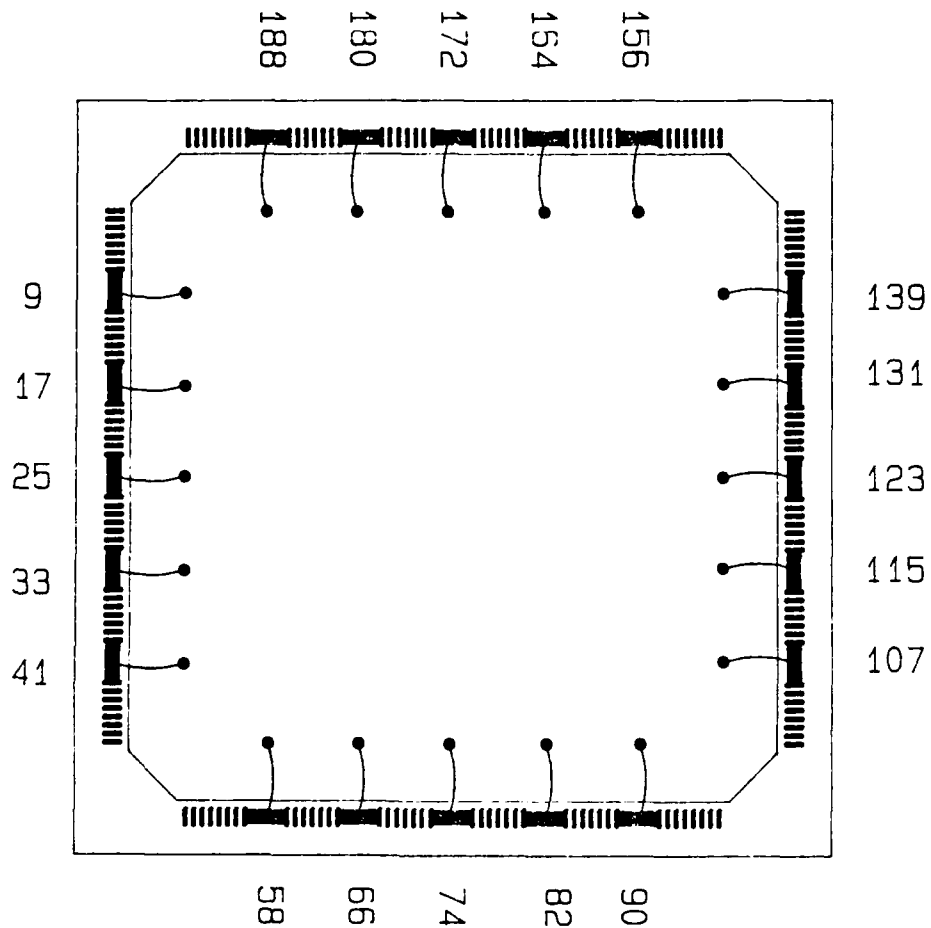


Figure 1.

**TEXAS**  
**INSTRUMENTS**  
Dallas, Texas

DWN DATE

ISSUE DATE

SIZE

**A**

FSCM NO

**96214**

DRAWING NO

2437700

REV

SCALE

SHEET 5

F-41

LABCOM 196-PIN PACKAGE  
MAXIMUM CURRENT DESTRUCTIVE TEST

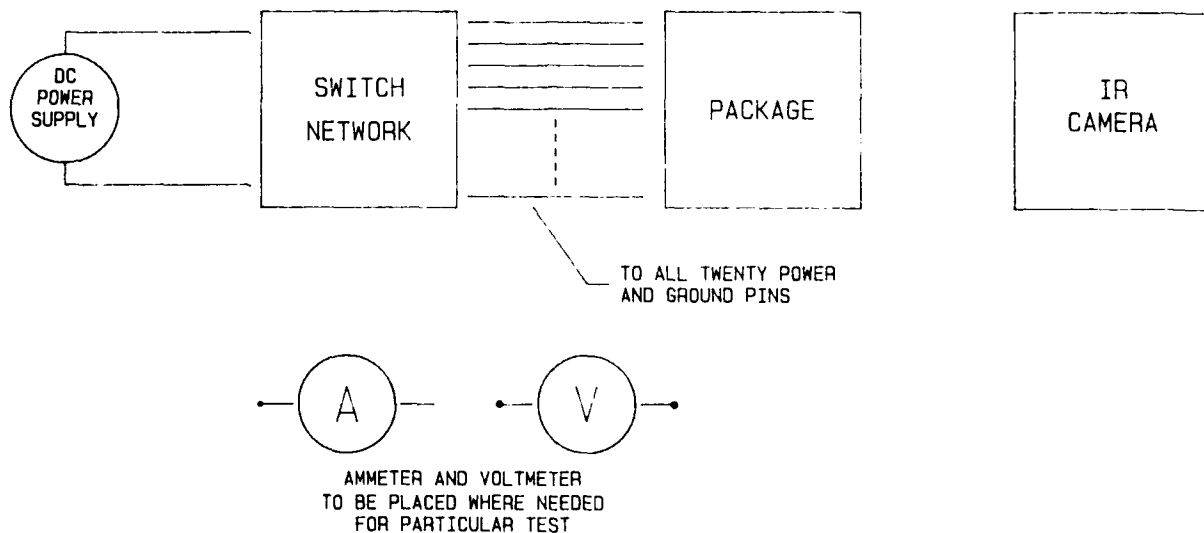


Figure 2.

<b>TEXAS INSTRUMENTS</b> <small>Dallas, Texas</small>	DWN	DATE	SIZE	FSCM NO	DRAWING NO	REV
	ISSUE DATE		A	96214	2437700	
			SCALE	SHEET		6

APPENDIX G  
TEST DESIGN DOCUMENT

<u>Page</u>	<u>Description</u>
G-2 - G-18	Test Design Document for Very High Speed Integrated Circuit

I I I I I I I I I I  
I I I I I I I I I I  
I I I I I I I I I I

SSSS	RRRR	AAA	M	M
S	R R	A A	MM	MM
S	R R	A A	M M	M
SSS	RRRR	A A	M	M
S	R R	AAAAA	M	M
S	R R	A A	M	M
SSSS	R R	A A	M	M

TTTTT	DDDD	DDDD	;;	222	222
T	D	D	D	;;	2 2 2 2
T	D	D	D		2 2
T	D	D	D	;;	2 2
T	D	D	D	;;	2 2
T	D	D	D	;	2 2
..	T	DDDD	DDDD	;	22222 22222

Job SRAM (26) queued to PR1 on 21-JAN-1988 08:46 by user MCHORSE, UIC  
[G210,MCHORSE], under account PROD\_ENG at priority 100, started on printer  
EXGEFESLPA0: on 21-JAN-1988 08:46 from queue PR1.

I I I I I I I I I I  
I I I I I I I I I I  
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TEST DESIGN DOCUMENT  
FOR  
VERY HIGH SPEED INTEGRATED CIRCUIT (VHSIC)  
SLC2189  
72K STATIC RAM

## 1.0 SCOPE

### 1.1 Identification

This specification describes the detailed design for the computer software programs identified as Colt III Test programs for the VHSIC 72k SRAM device.

### 1.2 Functional Summary

Each test program shall test the intended device functionally, and verify the DC and AC parametrics defined in the device specification.

## 2.0 REFERENCED DOCUMENTS

### 2.1 Government Documents

There are no applicable government documents.

### 2.2 Non-Government Documents

#### 2.2.1 Device Specifications

VHSIC SRAM Beta Test

#### 2.2.2 Business Development Quality Operating Instructions (QOI)

#### 2.2.3 Other

9299-3, Rev A Colt III Software Manual



### 3.0 PROGRAM IDENTIFICATION

3.1 This specification defines the requirements for the identification of the COLT III - AUTOMATIC TEST PROGRAM used as a Final Test on the VHSIC 72k SRAM.

3.1.1 Program Name :F2189.XXX

3.1.1.1 Extension

The extension XXX of program F2189.XXX is defined as the month and day of the latest revision. The months are 1-9 O,N,D (January - September October, November, December)

EX: F2189.623-----last revision June 23  
F2189.N17-----last revision November 17

3.1.2 Program Language

COLT Test System programming LANGUAGE (TSLANG) version 5.0

3.1.3 Operating System

COLT Operating System (COS)

3.1.4 Computer System

8088 Microprocessor control computer

#### 4. PROGRAM STRUCTURE

##### 4.1 Design Structure

###### 4.1.1 Program Description

###### MAIN PROGRAM

PINLIST AND LAYOUT  
OUTPUT AND TESTFLOW SETUP

###### TEST GROUPS

TEST GROUP 10 ---CONTINUITY  
TEST GROUP 20 ---INPUT LEAKAGE  
21 -----LEAKAGE  
22 -----LEAKAGE RESET PIN 0 AND 5 VOLTS  
TEST GROUP 30 ---PARAMETRIC TESTS  
31 -----POWER UP WITH RESET LO  
32 -----POWER UP WITH RESET HI  
33 -----POWER UP WITH CS LO  
34 -----POWER UP WRITE CYCLE  
35 -----POWER UP READ CYCLE  
TEST GROUP 40 ---OUTPUT LEAKAGE  
41 -----VOL AT IOL = - 8 ma  
42 -----VOH AT IOH = 4 ma  
TEST GROUP 50 ---NON PIPE CONTROL RAM TESTS  
51 -----PIPE BIT STUCK HIGH TEST  
52 -----CONTROL RAM FUNCTIONAL TEST  
TEST GROUP 60 ---NON PIPE MEMORY TESTS  
61 -----MEMORY FUNCTIONAL TEST  
TEST GROUP 70 ---PIPELINE CONTROL RAM TESTS  
71 -----NONPIPE TO PIPE TRANSITION  
72 -----CONTROL RAM FUNCTIONAL TEST  
TEST GROUP 80 ---PIPELINE MEMORY TESTS  
81 -----MEMORY FUNCTIONAL TEST

###### SUBROUTINES

PART BINNING (LABEL BINPART)  
VOLTAGE CONTROL AND TEMPERATURE (LABEL SETVALUES)  
PRINT STRINGS (LABEL SAVSTR)  
PRINT PARAMETRIC VALUES (LABEL PRIPARA)  
PRINT TWO BLANK LINES (LABEL BLKLN)  
RELAY CONTROL (LABELS VON & VOFF)  
LOAD RELAY CONTROL (LABELS VLOAD-ON & VLOAD-OFF)  
MAXIMUM VOLTAGE (LABEL LEVMAX)  
MINIMUM VOLTAGE (LABEL LEVMIN)  
NOMINAL VOLTAGE (LABEL LEVNOM)  
SUMMARY STATEMENT (LABEL SUMMARY:STATEMENT)  
SUMMARY CONTROL (LABEL SUMMARY)

LOOSE TIMING (LABEL GROSST)  
 NON PIPE 40 NS ACCESS TIME VALUES (LABEL NPACC40)  
 NON PIPE 50 NS ACCESS TIME VALUES (LABEL NPACC50)  
 NON PIPE 60 NS ACCESS TIME VALUES (LABEL NPACC60)  
 NON PIPE 70 NS ACCESS TIME VALUES (LABEL NPACC70)  
 PIPELINE 40 NS ACCESS TIME VALUES (LABEL NPACC40)  
 PIPELINE 50 NS ACCESS TIME VALUES (LABEL NPACC50)  
 PIPELINE 60 NS ACCESS TIME VALUES (LABEL NPACC60)  
 PIPELINE 70 NS ACCESS TIME VALUES (LABEL NPACC70)  
 TIMING SETUP VALUES PIPELINE & NON PIPE  
 (LABEL TIMING:SETUP)  
 TIMING MODIFICATIONS FOR PIPELINE SETUP & HOLD  
 (LABEL PL:SETUP:MOD)  
 (LABEL PL:HOLD:MOD)  
 PIPELINE TIMEING EDGE DEFINITIONS (LABEL PIPELINE:EDGE)  
 MEMORY TIMING BALUES (LABEL MEMORY:TIMING)  
 RESET PATTERN (LABEL RESET)  
 PARAMETRIC PATTERNS (LABEL PARA:PAT)  
 VOL VOH PATTERNS (LABEL VOLVOH:PAT)  
 NONPIPE CONTROL RAM PATTERNS (LABEL CNRAM:PAT)  
 NONPIPE MEMORY PATTERNS (LABEL NPMEM:PAT)  
 PIPELINE CONTROL RAM PATTERNS (LABEL PCNRAM:PAT)  
 PIPELINE MEMORY PATTERNS (LABEL PLMEM:PAT)  
 CONTROL RAM ADDRESSING (LABEL CNRAM:ADDR)  
 TIME SET 0 EDGE DEFINITIONS (LABEL TS0)  
 TIME SET 1 EDGE DEFINITIONS (LABEL TS1)  
 TIME SET 2 EDGE DEFINITIONS (LABEL TS2)  
 TIME SET 3 EDGE DEFINITIONS (LABEL TS3)  
 TIME SET 4 EDGE DEFINITIONS (LABEL TS4)  
 TIME SET 5 EDGE DEFINITIONS (LABEL TS5)  
 TIME SET 6 EDGE DEFINITIONS (LABEL TS6)  
 TIME SET 7 EDGE DEFINITIONS (LABEL TS7)  
 TIME SET 8 EDGE DEFINITIONS (LABEL TS8)

COLT TESTER PIN

COLT TESTER NAME

DEVICE PIN NAME

V V V V V V V V

SHIELD DPS1 VSS 1\_\_

J1-14 DPS2F\ 2\_\_

J1-15 DPS2S-VCC 3\_\_

J4-15 AY2 A11 4\_\_

J4-16 AY3 A12 5\_\_

J5- 1 DATA1 DQ0 6\_\_

J5- 2 DATA2 DQ1 7\_\_

J5- 3 DATA3 DQ2 8\_\_

J5- 4 DATA4 DQ3 9\_\_

J5- 9 DATA9 DQ8/P 10\_\_

J5- 8 DATA8 DQ7 11\_\_

J5- 7 DATA7 DQ6 12\_\_

J5- 6 DATA6 DQ5 13\_\_

J5- 5 DATA5 DQ4 14\_\_

J4- 8 AY1 A10 15\_\_

J4-14 AY0 A9 16\_\_

J1-18 DPS4F\_VDD 17\_\_

J1-19 DPS4S/ 18\_\_

32 A0 AX5 J4-11

31 \*PV DATA10 J5-10

30 A1 AX6 J4- 5

29 A2 AX7 J4- 6

28 A3 AX1 J4- 2

27 CT0 CLK5 J2-18

26 CT1 CLK4 J2-17

25 CT2 CLK3 J2-16

24 CLK/WE CLK1 J2-14

23 \*CS CLK2 J2-15

22 \*RST CLK6 J2-19

21 A8 AY4 J4-10

20 A7 AX0 J4- 1

19 A6 AX2 J4- 9

18 A5 AX3 J4- 3

17 A4 AX4 J4- 4

## 4.2 Constant and Array Definitions

### 4.2.1 Arrays

PARRY [INDEX,INDEX] = [0-2,0-4] holds parametric values  
DATAV [INDEX] = [0-8] holds voh-vol values of data  
pins for min and max testing

### 4.2.2 Constants

#### 4.2.2.1 DC Power Supply Parameters

VLOAD = 5.0 V

#### 4.2.2.2 DC Input Test Parameters

VIL = 0.0 V

VIH = 4.5 V

VOL = 1.5 V

VOH = 1.5 V

VREF = 1.5 V

#### 4.2.2.3 AC Parameters

##### 4.2.2.3.1 Non-Pipeline Control Ram

NPCWEPW = 18 ns  
 NPCADDRSUWR = 10 ns  
 NPCCSSUWR = 30 ns  
 NPCCTSUWR = 12 ns  
 NPCDATASUWR = 14 ns  
 NPCADDRHDWR = 3 ns  
 NPCCSHDWR = 0 ns  
 NPCCTHDWR = 0 ns  
 NPCDATAHDWR = 0 ns

##### 4.2.2.3.2 Non-Pipeline Main Memory

**NPMWEPW = 31 ns**  
 NPMADDRSUWR = 11 ns  
 NPMCSSUWR = 20 ns  
 NPMCTSUWR = 17 ns  
 NPMDATASUWR = 26 ns  
 NPMADDRHDWR = 0 ns  
 NPMCSHDWR = 0 ns  
 NPMCTHDWR = 0 ns  
 NPMDATAHDWR = 0 ns

##### 4.2.2.3.3 Pipeline Control Ram

	Setup Test	Hold Test
	-----	-----
PLCCLKACC =	56 ns	56 ns
PLCLKLOPW =	36 ns	36 ns
PLCADDRSU =	13 ns	35 ns
PLCCSSU =	10 ns	35 ns
PLCCTSU =	10 ns	35 ns
PLCDATASU =	14 ns	35 ns
PLCADDRHD =	35 ns	3 ns
PLCCSHD =	35 ns	3 ns
PLCCTHD =	35 ns	3 ns
PLCDATAHD =	35 ns	0 ns

##### 4.2.2.3.4 Pipeline Main Memory

	Setup Test	Hold Test
	-----	-----
PLMCKLOPW =	36 ns	36 ns
PLMADDRSU =	17 ns	35 ns
PLMCSSU =	10 ns	35 ns
PLMCTSU =	10 ns	35 ns
PLMDATASU =	25 ns	35 ns
PLMADDRHD =	35 ns	3 ns
PLMCSDH =	35 ns	3 ns
PLMCTHD =	35 ns	3 ns
PLMDATAHD =	35 ns	3 ns

## 5. PROGRAM FUNCTIONAL DESIGN

### 5.1 CONTINUITY TEST

- 5.1.1 Definition: This is the D.C. parametric test used to verify electrical continuity between the tester and each device pin.

**Colt Test Procedure:** Ground all power supplies, all input pins, and all output pins. Connect the Colt PMU to each active device pin, in turn, and force it to source 100 micro-amps of current. This causes a negative voltage at the device pin which should indicate the presence of a body effect diode (i.e.  $-0.5$  to  $-0.7$  volt drop). Any measurement greater than  $-0.01$  v is considered to indicate a short on the device pin and any measurement less than  $-1.5$  v indicates an open to the device pin. If the test is performed on a handler socket an initial failure will cause the handler socket to open and close and retest the part. A second failure will fail the part. This test is not related to any device specification.

- 5.1.2 Expected Inputs: None

- 5.1.3 Expected Outputs: Formatted listing of each pin in the continuity pin test set (NAME ALL statement), with it's corresponding voltage reading and the pass/fail status.

- 5.1.4 Program Label: CONT

- 5.1.5 Test Group Number: 10

### 5.2 INPUT LEAKAGE TEST

- 5.2.1 Definition: The input leakage current into an input when a minimum level 'low' voltage and a maximum level 'high' voltage is applied to that input.

**Colt Test Procedure:**

5.2.1.1 **IiL TEST:** With Vcc and Vdd applied to the part, all inputs forced to 5.5 v and Reset pin forced to 0.0 v, each input pin (except DQ's) in turn is disconnected from 5.5 v, connected to the Colt PMU, forced to 0.0 v and the leakage current measured. Leakage current less than  $-1$  micro-amp is considered a failure. Next all DQ's are disconnect from 5.5 v and connected (ganged) to Colt PMU. The PMU is forced to 0.0 v and total DQ leakage current is measured and leakage current less than  $-1$  micro-amp is considered a failure.

5.2.1.2 **Ii TEST:** With Vcc and Vdd applied to the part, all inputs forced to 0.0 v and Reset pin forced to 0.0 v, each input pin (except DQ's) in turn is disconnected from 0.0 v, connected to the Colt PMU, forced to 5.5 v and the leakage current measured. Leakage current greater than 10 micro-amp is considered a failure. Next all DQ's are disconnect from 0.0 v and connected (ganged) to Colt PMU. The PMU is forced to 5.5 v and total DQ leakage current is measured and leakage current greater than 1 micro-amp

is considered a failure.

5.2.1.3 IiL TEST (Reset Pin) : With Vcc and Vdd applied to the part, CS forced to 0.0 v the reset pin is connected to the Colt PMU, forced to 0.0 v and the leakage current measured. Leakage current less than -10 micro-amp is considered a failure.

5.2.1.4 Ii TEST (Reset Pin) : With Vcc and Vdd applied to the part, CS forced to 0.0 v the reset pin is connected to the Colt PMU, forced to 5.5 v and the leakage current measured. Leakage current greater than 10 micro-amp is considered a failure.

5.2.2 Expected Inputs: None

5.2.3 Expected Outputs: Formatted listing of each pin in the input leakage test sets (ADDX, ADDY, CLKS, DQS) with its corresponding current reading and the pass/fail status.

5.2.4 Program Label: INLEAK

5.2.5 Test Group Numbers: 20, 21, 22

5.2.6 Special Note: Testing is not discontinued for leakage failures.

### 5.3 PARAMETRIC CURRENT TEST

5.3.1 Definition: This is the D.C. parametric test used to verify specification standby and active currents, Icc and Idd.

#### Colt Test Procedure:

5.3.1.1 Reset-Pin-Low Test (Standby Current): The part is powered up at Vcc max (5.5 v) and Vdd max (3.6 v) and load resistors are attached to all DQ's. All inputs are forced to level indicated by parametric patterns (PARAPAT). While part is executing continuous reset-low patterns using loose timing (GROSST time set), Icc and Idd are measured. Currents of Idd greater than 10 ma Idd greater than 30 ma are considered failures.

5.3.1.2 Reset-Pin-High Test (Standby Current): The part is powered up at Vcc max (5.5 v) and Vdd max (3.6V) and load resistors are attached to all DQ's. All inputs are forced to level indicated by parametric patterns (PARAPAT). While part is executing continuous reset-high patterns using loose timing (GROSST time set), Icc and Idd are measured. Currents of Idd greater than 10 ma Idd greater than 30 ma are considered failures.

5.3.1.3 CS-Low Test (Active Current): The part is powered up at Vcc max (5.5 v) and Vdd max (3.6 v) and load resistors are attached to all DQ's. All inputs are forced to level indicated by parametric patterns (PARAPAT). While part is executing continuous CS-low pattern using loose timing (GROSST time set), Icc and Idd are measured. Currents of Idd greater than 10 ma Idd greater than 150 ma



are considered failures.

5.3.1.4 Memory-Write Test (Active Current): The part is powered up at Vcc max (5.5 v) and Vdd max (3.6 v) and load resistors are attached to all DQ's. All inputs are forced to level indicated by parametric patterns (PARAPAT). While part is executing continuous write checkerboard pattern using loose timing (GROSST time set), Icc and Idd are measured. Currents of Idd greater than 10 ma Idd greater than 150 ma are considered failures.

5.3.1.5 Memory-Read Test (Active Current): The part is powered up at Vcc max (5.5 v) and Vdd max (3.6 v) and load resistors are attached to all DQs. All inputs are forced to the level indicated by parametric patterns (PARAPAT). While part is executing continuous read checkerboard pattern using loose timing (GROSST time set). Icc and Idd are measured. Currents of Idd greater than 10 ma Idd greater than 150 ma are considered failures.

5.3.2 Expected Inputs: PARAPAT pattern set

5.3.3 Expected Outputs: Formatted Listing of the results of DC parametric test with a pass fail status.

5.3.4 Program Label: PARAM

5.3.5 Test Group Numbers: 30, 31, 32, 33, 34, 35

5.3.6 Special Note: Testing is not discontinued for parametric current failures.

#### 5.4 OUTPUT LEAKAGE TEST

##### 5.4.1 Definition:

5.4.1.1 VOL Definition: The voltage at an output terminal when the input conditions are such that a low level should exist at the output.

5.4.1.2 VOH Definition: The voltage at an output terminal when the input conditions are such that a high level should exist at the output.

Colt Test Procedure: The part is initially tested with the VOLVOH:PAT pattern set using 70 ns access time sets. If parts fail this initial test the VOL-VOH measurements are bypassed and a "MEMORY FAIL VOL-VOH SETUP" is printed on the crt. If the part passes this initial test the VOL-VOH measurements are taken. Each DQ individually is forced to - 8 ma while running the VOL patterns. Measurements for each DQ are stored in a data array. After the VOL measurements the maximum reading is saved for the VOL measurement. Next each DQ individually is forced to 4 ma while running the voh patterns. Measurements for each DQ are stored in a data array. After the voh measurements the minimum reading is saved for the voh measurement.

5.4.2 Expected Inputs: VOLVOH:PAT pattern set

5.4.3 Expected Outputs: Formatted listing of the results of the vol-voh test.

5.4.4 Program Label: OUTLEAK

5.4.5 Test Group Numbers: 40, 41, 42

5.4.6 Special Note: Testing is not discontinued for parametric current failures.

## 5.5 NONPIPELINE CONTROL RAM TESTS

5.5.1 Definition: This is the test that verifies the functionality and speed specification for the Non-pipeline Control Ram operations.

Colt Test Procedure: Three predetermined patterns were used to exercise the device and check for 1.) pipebit stuck high, 2.) functionality, and 3.) functionality at specified speed. All patterns are run at 5 mhz. The patterns used for functionality at speed have clock edges set 1 ns. faster than specified speed or at specified speed. A failure in any of the three patterns will abort the test with an appropriate fail message. Testing is performed at worst case Vcc and Vdd unless specified otherwise.

5.5.2 Expected Inputs: CNRAM:PAT pattern set.

5.5.3 Expected outputs: Pattern set ID and pass/fail status.

5.5.4 Program Label: CNRAM:TEST

5.5.5 Test Group Numbers: 50,51,52

5.5.6 Special Note: None

## 5.6 NONPIPELINE MAIN MEMORY TESTS

5.6.1 Definition: This is the test that verifies the functionality and speed specifications for the Non-pipeline memory operation.

Colt Test Procedure: Two predetermined patterns are used to exercise the device and check for functionality and functionality at specified speeds. All patterns are run at 5 mhz. The basic functionality pattern is a read-modify-write pattern. The patterns used for functionality at speed have clock edges set 1 ns. faster than specified speed or at specified speed. The patterns used for speed tests are a checkerboard and the parts are sorted into 50 ns, 60 ns, and 70 ns parts. A failure during the functionality tests or the 70 ns speed test will abort the the test with an appropriate fail message. A failure during the 60 ns or 50 ns speed test will sort the part according to the fastest speed passed and also give an appropriate message. Testing is performed at worst case Vcc and Vdd unless specified otherwise.

- 5.6.2 Expected Inputs: NPMEM:PAT pattern set.
- 5.6.3 Expected outputs: Pattern set ID and pass/fail status.
- 5.6.4 Program Label: MEM:TEST
- 5.6.5 Test Group Numbers: 60,61
- 5.6.6 Special Note: None

#### 5.7 PIPELINE CONTROL RAM TESTS

- 5.7.1 Definition: This is the test that verifies the functionality and speed specifications for the Pipeline Control Ram operations.

Colt Test Procedure: Two predetermined patterns are used to exercise the device and check for 1.) conversion to pipeline mode and 2.) functionality and functionality at specified speed. All patterns are run at 5 mhz. The patterns used for functionality at speed have clock edges set 1 ns. faster than specified speed or at specified speed. A failure in either of the two patterns will abort the test with an appropriate fail message. Testing is performed at worst case Vcc and Vdd unless specified otherwise.

- 5.7.2 Expected Inputs: PCNRAM:PAT pattern set.
- 5.7.3 Expected outputs: Pattern set ID and pass/fail status.
- 5.7.4 Program Label: PCNRAM:TEST
- 5.7.5 Test Group Numbers: 70,71,72
- 5.7.6 Special Note: None

#### 5.8 PIPELINE MAIN MEMORY TESTS

- 5.8.1 Definition: This is the test that verifies the functionality and speed specifications for the Pipeline memory operation.

Colt Test Procedure: Two predetermined patterns are used to exercise the device and check for functionality at specified speeds. All patterns are run at 5 mhz. The basic functionality pattern is a read-modify-write pattern. The patterns used for functionality at speed have clock edges set 1 ns. faster than specified speed or at specified speed. The patterns used for speed tests are a checkerboard and the parts are sorted into 50 ns, 60 ns, and 70 ns parts. A failure during the functionality tests or the 70 ns speed test will abort the test with an appropriate fail message. A failure during the 60 ns or 50 ns speed test will sort the part

according to the fastest speed passed and also give an appropriate message. Testing is performed at worst case Vcc and Vdd unless specified otherwise.

5.8.2 Expected Inputs: PLMEM:PAT pattern set.

5.8.3 Expected outputs: Pattern set ID and pass/fail status.

5.8.4 Program Label: PLMEM:TEST

5.8.5 Test Group Numbers: 80,81

5.8.6 Special Note: None

## 6. PROGRAM REQUIREMENTS

### 6.1 Requirements Traceability Matrix

*****			
* PROGRAM REQUIREMENTS	* TDD PARAGRAPH	* SPEC CONTROL	* DRAWING
*****			
* 1. Voh	* 5.4	* TABLE 1	* *
* 2. Vol	* 5.4	* TABLE 1	* *
* 3. Ii	* 5.2	* TABLE 1	* *
* 4. Iil	* 5.2	* TABLE 1	* *
* 5. Icc5	* 5.3	* TABLE 1	* *
* 6. Icc3 Idle	* 5.3	* TABLE 1	* *
* 7. Icc3 Active	* 5.3	* TABLE 1	* *
* Pipeline Mode Memory Cycle	*	*	*
* 8. Tasuc	* 5.8	* TABLE 1	* *
* 9. Tcsuc	* 5.8	* TABLE 1	* *
* 10. Tctc	* 5.8	* TABLE 1	* *
* 11. Tdsuc	* 5.8	* TABLE 1	* *
* 12. Tahc	* 5.8	* TABLE 1	* *
* 13. Tchc	* 5.8	* TABLE 1	* *
* 14. Tcth	* 5.8	* TABLE 1	* *
* 15. Tdhc	* 5.8	* TABLE 1	* *
* 16. Twpc	* 5.8	* TABLE 1	* *
*****			

* 17. Tdc Dev 01	* 5.8	* TABLE 1	*
* 18. Tdc Dev 02	* 5.8	* TABLE 1	*
* Pipeline Mode Control Cycle			
* 19. Tasuc	* 5.7	* TABLE 1	*
* 20. Tcsuc	* 5.7	* TABLE 1	*
* 21. Tctc	* 5.7	* TABLE 1	*
* 22. Tdsuc	* 5.7	* TABLE 1	*
* 23. Tahc	* 5.7	* TABLE 1	*
* 24. Tchc	* 5.7	* TABLE 1	*
* 25. Tcth	* 5.7	* TABLE 1	*
* 26. Tdhc	* 5.7	* TABLE 1	*
* 27. Tdc	* 5.7	* TABLE 1	*
* Non-pipeline Memory cycle			
* 28. Tdacs	* 5.6	* TABLE 1	*
* 29. Tdaa	* 5.6	* TABLE 1	*
* 30. Tdac	* 5.6	* TABLE 1	*
* 31. Tas	* 5.6	* TABLE 1	*
* 32. Tds	* 5.6	* TABLE 1	*
* 33. Tah	* 5.6	* TABLE 1	*
* 34. Tdh	* 5.6	* TABLE 1	*
* 35. Twp	* 5.6	* TABLE 1	*
* Non-pipeline Control Cycle			
* 36. Tas	* 5.5	* TABLE 1	*
* 37. Tds	* 5.5	* TABLE 1	*
* 38. Tah	* 5.5	* TABLE 1	*
* 39. Tdh	* 5.5	* TABLE 1	*
* 40. Tcs	* 5.5	* TABLE 1	*
* 41. Tch	* 5.5	* TABLE 1	*
* 42. Tdaa	* 5.5	* TABLE 1	*
* 43. Tdac	* 5.5	* TABLE 1	*
* 44. Twp	* 5.5	* TABLE 1	*
*****			

## 6.2 Software Test Philosophy

The purpose of the F2189.XXX Test Software is to test the minimum requirements of the SLC2189 device. The software will be executed on a device; at -55, 25, or 125 degrees centigrade; with the COLT III Memory Tester and the DELTA OP2A Environmental Handler. A continuity test is first performed to ensure that there is adequate contact between the device and the test setup. DC parametrics are first performed followed by AC functional tests. Parts are sorted at the handler according to their conformance to the Mil Drawing Specifications.

## 6.3 Program Operating Environment

<u>SOFTWARE</u>	<u>MANUFACTURER</u>	<u>PART NO.</u>	<u>REV.</u>
COLT Test System Programming Language (TSLANG)	Pacific Western		5.0
Final Acceptance Test Program SLC2189			

## 6.4 Hardware Requirements

<u>HARDWARE</u> -----	<u>MANUFACTURER</u> -----	<u>PART NO.</u> -----
Automatic Test Equipment	Pacific Western	COLT III
Environmental Handler	Delta Design, Inc.	DELTA-OP2A
Test Station Interface (TSI)		
Handler Control Cable (HCI)		

APPENDIX H  
AC PARAMETRIC TEST RESULTS

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H-2 - H-9	AC Parametric Test Results

## APPENDIX H

### AC PARAMETRIC TEST RESULTS

#### NONPIPE CONTROL RAM DATA

```

----READ CYCLE DATA----
      (Tdac)   CT1 ACCESS      = 25.5  NS
              CS ACCESS      = 31.25 NS
      (Tdaa)   ADD ACCESS      = 24.0  NS
      (Tdac)   CT2 ACCESS      = 9.5   NS
      (Tdd)    CT1 DISABLE     = 19.75 NS
              CS DISABLE     = 838.0  NS
      (Tdd)    CT2 DISABLE     = 21.25 NS
----WRITE CYCLE DATA----
      (Tds)    *WE DATA SETUP = 7.25  NS
      (Tdh)    *WE DATA HOLD  = -3.0  NS
      (Twp)    *WE MIN WIDTH   = 13.5  NS
      (Tas)    *WE ADD SETUP   = -14.25 NS
      (Tcs)    *WE CT1 SETUP   = -21.0  NS
      (Tah)    *WE ADD HOLD    = -6.5   NS
      (Tch)    *WE CT1 HOLD    = -18.5  NS

```

#### NONPIPE MAIN MEMORY DATA

##### VIL-VIH MEASUREMENTS

	VIL(max)	VIS(min)
ADDRESS LINES	1.216 V	1.595 V
DATA LINES	1.482 V	1.773 V
CONTROL LINES	1.014 V	1.473 V

```

----READ CYCLE DATA----
      (Tdac)   CT2 ACCESS      = 14.0  NS
              CS ACCESS      = 47.25 NS
      (Tdaa)   ADD ACCESS      = 45.5  NS
      (Tden)   DATA OUTPUT ENABLE = 56.25 NS
      (Tdd)    CT2 DISABLE     = 18.0  NS
              CS DISABLE     = 28.25 NS
      (Tdz)    CS DISABLE     = 24.0  NS
----WRITE CYCLE DATA----
      (Tds)    *WE DATA SETUP = 19.75 NS
              *CS DATA SETUP = 19.25 NS
      (Tdh)    *WE DATA HOLD  = -5.0  NS
              *CS DATA HOLD  = -5.0  NS
      (Twp)    *WE MIN WIDTH   = 21.5  NS
              *CS MIN WIDTH   = 29.0  NS
      (Tas)    *WE ADD SETUP   = -17.5  NS
              *CS ADD SETUP   = -28.75 NS
      (Tah)    *WE ADD HOLD    = -17.75 NS
              *CS ADD HOLD    = -17.75 NS

```



# PIPELINE CONTROL RAM DATA

## ----READ CYCLE DATA----

(Tdc)	CLK ACCESS	=	36.0	NS
(Tdhc)	CLK DISABLE	=	18.0	NS
(Tasuc)	CLK ADD SETUP	=	15.25	NS
(Tahc)	CLK ADD HOLD	=	-10.25	NS
(Tcsuc)	CLK CS SETUP	=	19.75	NS
(Tchc)	CLK CS HOLD	=	-17.75	NS
(Tctc)	CLK CT1 SETUP	=	14.5	NS
(Tcth)	CLK CT1 HOLD	=	-10.0	NS
(Tctc)	CLK CT2 SETUP	=	12.0	NS
(Tcth)	CLK CT2 HOLD	=	-9.75	NS

## ----WRITE CYCLE DATA----

(Tasuc)	CLK ADD SETUP	=	16.0	NS
(Tahc)	CLK ADD HOLD	=	-9.75	NS
(Tcsuc)	CLK CS SETUP	=	19.0	NS
(Tchc)	CLK CS HOLD	=	-18.0	NS
(Tctc)	CLK CT1 SETUP	=	14.0	NS
(Tcth)	CLK CT1 HOLD	=	-10.25	NS
(Tdsuc)	CLK DATA SETUP	=	7.25	NS
(Tdhw)	CLK DATA HOLD	=	-3.0	NS

# PIPELINE MAIN MEMORY DATA

## ----READ CYCLE DATA----

(Tdc)	CLK DATA ACCESS	=	49.75	NS
(Tdhc)	CLK DATA HOLD	=	13.0	NS
(Tasuc)	CLK ADD SETUP	=	15.5	NS
(Tahc)	CLK ADD HOLD	=	-9.5	NS
(Tcsuc)	CLK CS SETUP	=	18.75	NS
(Tchc)	CLK CS HOLD	=	-17.5	NS
(Tctc)	CLK CT2 SETUP	=	11.25	NS
(Tcth)	CLK CT2 HOLD	=	-9.0	NS
(Tden)	DATA OUTPUT ENABLE	=	18.75	NS
(Tdz)	DATA OUTPUT HI-Z	=	13.0	NS

## ----WRITE CYCLE DATA----

(Tasuc)	CLK ADD SETUP	=	17.75	NS
(Tahc)	CLK ADD HOLD	=	-9.0	NS
(Tcsuc)	CLK CS SETUP	=	19.75	NS
(Tchc)	CLK CS HOLD	=	-17.25	NS
(Tdsuc)	CLK DATA SETUP	=	17.75	NS
(Tdhw)	CLK DATA HOLD	=	-4.0	NS
(Twpc)	CLK LOW TIME	=	28.25	NS

Vcc = 5.0

Vdd = 3.3

TEMP = 0

#### NONPIPE CONTROL RAM DATA

##### ----READ CYCLE DATA----

(Tdac)	CT1 ACCESS	=	26.0	NS
	CS ACCESS	=	32.75	NS
(Tdaa)	ADD ACCESS	=	23.25	NS
(Tdac)	CT2 ACCESS	=	8.75	NS
(Tdd)	CT1 DISABLE	=	19.0	NS
	CS DISABLE	=	838.0	NS
(Tdd)	CT2 DISABLE	=	21.0	NS

##### ----WRITE CYCLE DATA----

(Tds)	*WE DATA SETUP	=	7.25	NS
(Tdh)	*WE DATA HOLD	=	-3.0	NS
(Twp)	*WE MIN WIDTH	=	14.0	NS
(Tas)	*WE ADD SETUP	=	-14.75	NS
(Tcs)	*WE CT1 SETUP	=	-20.0	NS
(Tah)	*WE ADD HOLD	=	-6.5	NS
(Tch)	*WE CT1 HOLD	=	-18.0	NS

#### NONPIPE MAIN MEMORY DATA

##### VIL-VIH MEASUREMENTS

	VIL(max)	VIS(min)
ADDRESS LINES	1.31 V	1.661 V
DATA LINES	1.569 V	1.839 V
CONTROL LINES	1.021 V	1.539 V

##### ----READ CYCLE DATA----

(Tdac)	CT2 ACCESS	=	13.5	NS
	CS ACCESS	=	46.25	NS
(Tdaa)	ADD ACCESS	=	43.75	NS
(Tden)	DATA OUTPUT ENABLE	=	52.0	NS
(Tdd)	CT2 DISABLE	=	18.25	NS
	CS DISABLE	=	29.5	NS
(Tdz)	CS DISABLE	=	24.75	NS

##### ----WRITE CYCLE DATA----

(Tds)	*WE DATA SETUP	=	19.25	NS
	*CS DATA SETUP	=	19.0	NS
(Tdh)	*WE DATA HOLD	=	-5.0	NS
	*CS DATA HOLD	=	-4.5	NS
(Twp)	*WE MIN WIDTH	=	21.75	NS
	*CS MIN WIDTH	=	23.0	NS
(Tas)	*WE ADD SETUP	=	-16.75	NS
	*CS ADD SETUP	=	-29.75	NS
(Tah)	*WE ADD HOLD	=	-17.75	NS
	*CS ADD HOLD	=	-18.25	NS

# PIPELINE CONTRAL RAM DATA

(Tdc)	CLK ACCESS	=	35.25 NS
(Tdhc)	CLK DISABLE	=	18.25 NS
(Tasuc)	CLK ADD SETUP	=	14.75 NS
(Tahc)	CLK ADD HOLD	=	-9.75 NS
(Tcsuc)	CLK CS SETUP	=	20.25 NS
(Tchc)	CLK CS HOLD	=	-19.0 NS
(Tctc)	CLK CT1 SETUP	=	13.25 NS
(Tcth)	CLK CT1 HOLD	=	-10.5 NS
(Tctc)	CLK CT2 SETUP	=	12.75 NS
(Tcth)	CLK CT2 HOLD	=	-9.75 NS

## ----WRITE CYCLE DATA----

(Tasuc)	CLK ADD SETUP	=	15.0 NS
(Tahc)	CLK ADD HOLD	=	-9.0 NS
(Tcsuc)	CLK CS SETUP	=	19.5 NS
(Tchc)	CLK CS HOLD	=	-19.5 NS
(Tctc)	CLK CT1 SETUP	=	13.25 NS
(Tcth)	CLK CT1 HOLD	=	-10.75 NS
(Tdsuc)	CLK DATA SETUP	=	7.25 NS
(Tdhw)	CLK DATA HOLD	=	-3.25 NS

# PIPELINE MAIN MEMORY DATA

## ----READ CYCLE DATA----

(Tdc)	CLK DATA ACCESS	=	44.75 NS
(Tdhc)	CLK DATA HOLD	=	13.5 NS
(Tasuc)	CLK ADD SETUP	=	15.5 NS
(Tahc)	CLK ADD HOLD	=	-9.5 NS
(Tcsuc)	CLK CS SETUP	=	19.5 NS
(Tchc)	CLK CS HOLD	=	-19.0 NS
(Tctc)	CLK CT2 SETUP	=	12.25 NS
(Tcth)	CLK CT2 HOLD	=	-9.75 NS
(Tden)	DATA OUTPUT ENABLE	=	18.0 NS
(Tdz)	DATA OUTPUT HI-Z	=	13.5 NS

## ----WRITE CYCLE DATA----

(Tasuc)	CLK ADD SETUP	=	16.0 NS
(Tahc)	CLK ADD HOLD	=	-9.5 NS
(Tcsuc)	CLK CS SETUP	=	20.0 NS
(Tchc)	CLK CS HOLD	=	-18.75 NS
(Tdsuc)	CLK DATA SETUP	=	17.25 NS
(Tdhw)	CLK DATA HOLD	=	-3.75 NS
(Twpc)	CLK LOW TIME	=	29.0 NS

Vcc = 5.0

Vdd = 3.3

TEMP = 0

# NONPIPE CONTROL RAM DATA

## ----READ CYCLE DATA----

(Tdac)	CT1 ACCESS	=	24.75 NS
	CS ACCESS	=	28.5 NS
(Tdaa)	ADD ACCESS	=	23.75 NS
(Tdac)	CT2 ACCESS	=	9.25 NS
(Tdd)	CT1 DISABLE	=	19.0 NS
	CS DISABLE	=	28.5 NS
(Tdd)	CT2 DISABLE	=	19.0 NS

## ----WRITE CYCLE DATA----

(Tds)	*WE DATA SETUP	=	7.5 NS
(Tdh)	*WE DATA HOLD	=	-3.25 NS
(Twp)	*WE MIN WIDTH	=	14.0 NS
(Tas)	*WE ADD SETUP	=	-14.75 NS
(Tcs)	*WE CT1 SETUP	=	-20.25 NS
(Tah)	*WE ADD HOLD	=	-6.75 NS
(Tch)	*WE CT1 HOLD	=	-17.75 NS

# NONPIPE MAIN MEMORY DATA VIL-VIH MEASUREMENTS

ADDRESS LINES	VIL(max)	VIS(min)
	0.685 V	1.557 V
DATA LINES	1.397 V	1.736 V
CONTROL LINES	1.021 V	1.539 V

## ----READ CYCLE DATA----

(Tdac)	CT2 ACCESS	=	9.75 NS
	CS ACCESS	=	44.25 NS
(Tdaa)	ADD ACCESS	=	917.0 NS
(Tden)	DATA OUTPUT ENABLE	=	937.0 NS
(Tdd)	CT2 DISABLE	=	16.25 NS
	CS DISABLE	=	26.25 NS
(Tdz)	CS DISABLE	=	22.5 NS

## ----WRITE CYCLE DATA----

(Tds)	*WE DATA SETUP	=	20.25 NS
	*CS DATA SETUP	=	19.75 NS
(Tdh)	*WE DATA HOLD	=	-4.75 NS
	*CS DATA HOLD	=	-4.5 NS
(Twp)	*WE MIN WIDTH	=	92.25 NS
	*CS MIN WIDTH	=	30.75 NS
(Tas)	*WE ADD SETUP	=	22.5 NS
	*CS ADD SETUP	=	-19.75 NS
(Tah)	*WE ADD HOLD	=	35.5 NS
	*CS ADD HOLD	=	-4.25 NS

# PIPELINE CONTROL RAM DATA

(Tdc)	CLK ACCESS	=	35.5 NS
(Tdhc)	CLK DISABLE	=	17.0 NS
(Tasuc)	CLK ADD SETUP	=	13.25 NS
(Tahc)	CLK ADD HOLD	=	-8.5 NS
(Tcsuc)	CLK CS SETUP	=	16.25 NS
(Tchc)	CLK CS HOLD	=	-15.25 NS
(Tctc)	CLK CT1 SETUP	=	11.75 NS
(Tcth)	CLK CT1 HOLD	=	-8.0 NS
(Tctc)	CLK CT2 SETUP	=	11.0 NS
(Tcth)	CLK CT2 HOLD	=	-7.75 NS

## ----WRITE CYCLE DATA----

(Tasuc)	CLK ADD SETUP	=	12.5 NS
(Tahc)	CLK ADD HOLD	=	-7.75 NS
(Tcsuc)	CLK CS SETUP	=	16.0 NS
(Tchc)	CLK CS HOLD	=	-15.5 NS
(Tctc)	CLK CT1 SETUP	=	11.25 NS
(Tcth)	CLK CT1 HOLD	=	-8.25 NS
(Tdsuc)	CLK DATA SETUP	=	7.75 NS
(Tdhw)	CLK DATA HOLD	=	-3.25 NS

# PIPELINE MAIN MEMORY DATA

## ----READ CYCLE DATA----

(Tdc)	CLK DATA ACCESS	=	46.5 NS
(Tdhc)	CLK DATA HOLD	=	13.0 NS
(Tasuc)	CLK ADD SETUP	=	13.75 NS
(Tahc)	CLK ADD HOLD	=	-8.0 NS
(Tcsuc)	CLK CS SETUP	=	16.0 NS
(Tchc)	CLK CS HOLD	=	-15.0 NS
(Tctc)	CLK CT2 SETUP	=	10.5 NS
(Tcth)	CLK CT2 HOLD	=	-7.25 NS
(Tden)	DATA OUTPUT ENABLE	=	14.75 NS
(Tdz)	DATA OUTPUT HI-Z	=	13.0 NS

## ----WRITE CYCLE DATA----

(Tasuc)	CLK ADD SETUP	=	14.0 NS
(Tahc)	CLK ADD HOLD	=	-7.75 NS
(Tcsuc)	CLK CS SETUP	=	16.25 NS
(Tchc)	CLK CS HOLD	=	-15.0 NS
(Tdsuc)	CLK DATA SETUP	=	17.75 NS
(Tdhw)	CLK DATA HOLD	=	-3.75 NS
(Twpc)	CLK LOW TIME	=	27.0 NS

Vcc = 5.0

Vdd = 3.3

TEMP = 0

#### NONPIPE CONTROL RAM DATA

##### ----READ CYCLE DATA----

(Tdac)	CT1 ACCESS	=	24.5	NS
	CS ACCESS	=	30.25	NS
(Tdaa)	ADD ACCESS	=	22.0	NS
(Tdac)	CT2 ACCESS	=	8.0	NS
(Tdd)	CT1 DISABLE	=	18.0	NS
	CS DISABLE	=	28.75	NS
(Tdd)	CT2 DISABLE	=	18.5	NS

##### ----WRITE CYCLE DATA----

(Tds)	*WE DATA SETUP	=	7.25	NS
(Tdh)	*WE DATA HOLD	=	-3.25	NS
(Twp)	*WE MIN WIDTH	=	14.0	NS
(Tas)	*WE ADD SETUP	=	-14.5	NS
(Tcs)	*WE CT1 SETUP	=	-20.25	NS
(Tah)	*WE ADD HOLD	=	-6.5	NS
(Tch)	*WE CT1 HOLD	=	-17.75	NS

#### NONPIPE MAIN MEMORY DATA VIL-VIH MEASUREMENTS

	VIL(max)	VIS(min)
ADDRESS LINES	1.303 V	1.689 V
DATA LINES	1.553 V	1.867 V
CONTROL LINES	1.021 V	1.529 V

##### ----READ CYCLE DATA----

(Tdac)	CT2 ACCESS	=	12.5	NS
	CS ACCESS	=	43.5	NS
(Tdaa)	ADD ACCESS	=	42.5	NS
(Tden)	DATA OUTPUT ENABLE	=	52.25	NS
(Tdd)	CT2 DISABLE	=	16.0	NS
	CS DISABLE	=	26.5	NS
(Tdz)	CS DISABLE	=	22.25	NS

##### ----WRITE CYCLE DATA----

(Tds)	*WE DATA SETUP	=	19.25	NS
	*CS DATA SETUP	=	18.75	NS
(Tdh)	*WE DATA HOLD	=	-4.75	NS
	*CS DATA HOLD	=	-4.5	NS
(Twp)	*WE MIN WIDTH	=	21.25	NS
	*CS MIN WIDTH	=	28.5	NS
(Tas)	*WE ADD SETUP	=	-16.25	NS
	*CS ADD SETUP	=	-27.5	NS
(Tah)	*WE ADD HOLD	=	-17.0	NS
	*CS ADD HOLD	=	-17.25	NS

# PIPELINE CONTRAL RAM DATA

(Tdc)	CLK ACCESS	=	34.25 NS
(Tdhc)	CLK DISABLE	=	17.0 NS
(Tasuc)	CLK ADD SETUP	=	13.25 NS
(Tahc)	CLK ADD HOLD	=	-9.0 NS
(Tcsuc)	CLK CS SETUP	=	17.25 NS
(Tchc)	CLK CS HOLD	=	-16.5 NS
(Tctc)	CLK CT1 SETUP	=	13.0 NS
(Tcth)	CLK CT1 HOLD	=	-8.75 NS
(Tctc)	CLK CT2 SETUP	=	11.25 NS
(Tcth)	CLK CT2 HOLD	=	-8.5 NS

## ----WRITE CYCLE DATA----

(Tasuc)	CLK ADD SETUP	=	13.5 NS
(Tahc)	CLK ADD HOLD	=	-8.5 NS
(Tcsuc)	CLK CS SETUP	=	16.5 NS
(Tchc)	CLK CS HOLD	=	-17.0 NS
(Tctc)	CLK CT1 SETUP	=	12.5 NS
(Tcth)	CLK CT1 HOLD	=	-9.0 NS
(Tdsuc)	CLK DATA SETUP	=	7.75 NS
(Tdhw)	CLK DATA HOLD	=	-3.25 NS

# PIPELINE MAIN MEMORY DATA

## ----READ CYCLE DATA----

(Tdc)	CLK DATA ACCESS	=	43.25 NS
(Tdhc)	CLK DATA HOLD	=	13.5 NS
(Tasuc)	CLK ADD SETUP	=	13.25 NS
(Tahc)	CLK ADD HOLD	=	-8.5 NS
(Tcsuc)	CLK CS SETUP	=	16.25 NS
(Tchc)	CLK CS HOLD	=	-16.5 NS
(Tctc)	CLK CT2 SETUP	=	11.0 NS
(Tcth)	CLK CT2 HOLD	=	-8.25 NS
(Tden)	DATA OUTPUT ENABLE	=	17.25 NS
(Tdz)	DATA OUTPUT HI-Z	=	13.5 NS

## ----WRITE CYCLE DATA----

(Tasuc)	CLK ADD SETUP	=	13.75 NS
(Tahc)	CLK ADD HOLD	=	-8.5 NS
(Tcsuc)	CLK CS SETUP	=	17.25 NS
(Tchc)	CLK CS HOLD	=	-16.25 NS
(Tdsuc)	CLK DATA SETUP	=	17.25 NS
(Tdhw)	CLK DATA HOLD	=	-3.75 NS
(Twpc)	CLK LOW TIME	=	27.0 NS

APPENDIX I  
DC PARAMETRIC TEST RESULTS

<u>Page</u>	<u>Description</u>
I-2	DC Parametric Test Results



# APPENDIX I

## DC PARAMETRIC TEST RESULTS

### INPUT LEAKAGE AT 0 VOLTS

AX1 = 0.032 NA	AY1 = 0.018 NA	CT1 = 0.002 NA	DQ1 = 0.194 $\mu a$
AX2 = 0.032 NA	AY2 = 0.002 NA	CT2 = 0.002 NA	DQ2 = 0.193 $\mu a$
AX3 = 0.002 NA	AY3 = 0.022 NA	CS = -2.048 NA	DQ3 = 0.191 $\mu a$
AX4 = 0.003 NA	AY4 = 0.002 NA	CLK = 0.002 NA	DQ4 = 0.022 $\mu a$
AX5 = 0.002 NA		RST = 0.007 NA	DQ5 = 0.157 $\mu a$
AX6 = 0.02 NA			DQ6 = 0.181 $\mu a$
AX7 = 0.016 NA			DQ7 = 0.021 $\mu a$
			DQ8 = -0.02 $\mu a$

### INPUT LEAKAGE AT VCC

AX1 = 0.062 NA	AY1 = 0.05 NA	CT1 = 0.005 NA	DQ1 = 0.292 $\mu a$
AX2 = 0.077 NA	AY2 = 0.005 NA	CT2 = 0.005 NA	DQ2 = 0.293 $\mu a$
AX3 = 0.005 NA	AY3 = 0.05 NA	CS = 0.005 NA	DQ3 = 0.29 $\mu a$
AX4 = 0.007 NA	AY4 = 0.005 NA	CLK = 0.003 NA	DQ4 = 0.035 $\mu a$
AX5 = 0.005 NA		RST = 0.017 NA	DQ5 = 0.238 $\mu a$
AX6 = 0.026 NA			DQ6 = 0.284 $\mu a$
AX7 = 0.036 NA			DQ7 = 0.035 $\mu a$
			DQ8 = 0.009 $\mu a$

### VOL AT - 8 MA

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	DQ8
VOLTS	-0.047	-0.047	-0.047	-0.047	-0.046	-0.046	-0.046	-0.047	-0.046
VOH AT	4MA								

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	DQ8
VOLTS	1.003	1.047	1.055	1.077	1.07	1.087	1.055	1.084	0.987

APPENDIX J

SLC2189 DATA SHEET

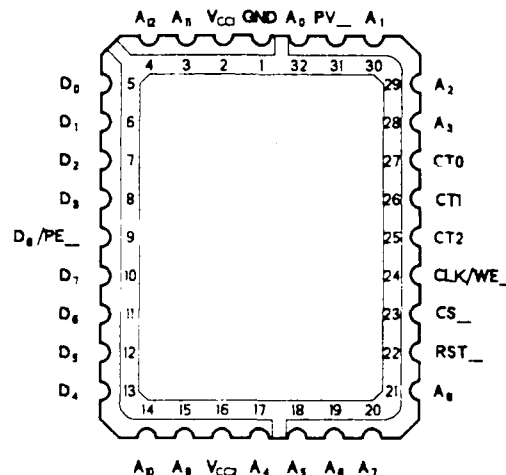
<u>Page</u>	<u>Description</u>
J-2 - J-15	SLC2189 Data Sheet

## ADVANCE INFORMATION

## SLC2189 8,192-WORD BY 9-BIT STATIC RAM

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- Static design eliminates refresh cycles and improves reliability.
- On-chip parity generation and checking logic.
- Built-in write-protection on 1K word boundaries.
  - CPU initiated write-protection
  - DMA initiated write-protection
- Two timing modes:
  - Pipelined (synchronous) operation
  - Conventional (asynchronous) non-pipelined operation
- Full TTL compatibility on all inputs and outputs.
- 32-pad high-density Leadless Ceramic Chip Carrier (LCC) Package.



### description

The SLC2189 is a single chip memory system containing 72K of SRAM, write protection and parity detection circuitry. This flexible device, along with other members of TI's System Level Component (SLC) family, is designed for use in high-performance military systems. The unique programmable machine cycle architecture of the SLC2189 allows it to be used in applications requiring pipelined operations, conventional discrete read and write type operations, or in systems requiring on-the-fly changes in memory accessing techniques. The SLC2189 employs state-of-the-art NMOS technology for very high speed performance. Static design is used throughout the device to eliminate refresh cycles and to improve system reliability. The device is packaged in a compact 32-pad Leadless Ceramic Chip Carrier with contact spacings on 0.050-inch centers.

The Static Random Access Memory (SRAM) is composed of high speed storage elements organized as an array of 8,192 9-bit words. The 9th bit of each word can be programmed for use as either a data memory bit or as a parity error bit.

A variety of programmable parity generation and checking functions allow system designers to implement sophisticated maintenance, test, error correction and recovery procedures. Parity bits are generated during write operations and are stored as the ninth bit of each word. Parity checking is done during read operations at which time the parity is recalculated and compared to the stored value. A logical 0 on pin D8/PE<sub>1</sub> indicates the detection of a parity error. During pipelined memory operations, the SLC2189 can also be programmed to report parity errors either in the same or subsequent clock cycle.

The write protection circuitry can be programmed to protect individual 1K blocks of memory. Two separate functions are provided to allow either CPU or DMA initiated write protection.

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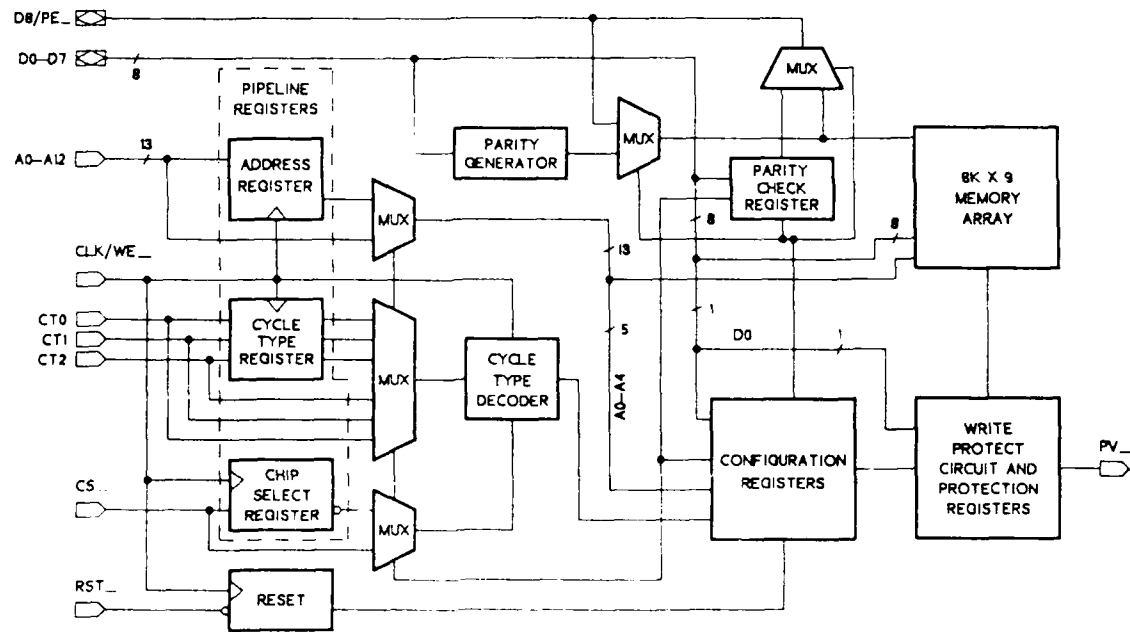
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SLC2189  
8,192-WORD BY 9-BIT STATIC RAM

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functional block diagram



operation

The SLC2189 is an SRAM that has been coupled with a dedicated memory controller. The memory controller monitors the control lines for new instructions, interprets them, and then executes a variety of machine cycles and/or device operations. At the beginning of each new machine cycle, control signals CT0-CT2, CS, and RST are sampled, decoded, and the device "reconfigured" to implement the new instruction. The various machine cycles are listed in Table 1 along with the control line settings for each.

In addition to the reconfigurable machine cycles, the SLC2189 can be programmed to perform one or more auxiliary memory functions along with its normal read and write operations. These include:

- Set DMA Write Protection on any 1K Block
- Set CPU Write Protection on any 1K Block
- Select Pipelined or Normal Accessing
- Set Same or Next Cycle Parity Reporting
- Set D8/PE Output Buffer to 3-State or Open-Drain Mode
- Read DMA Write Protection Status
- Read CPU Write Protection Status
- Read Memory Accessing Mode
- Read Parity Report Cycle Flag
- Read D8/PE Output Buffer Mode

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the address bus (pins A0 . . . A12)

SRAM memory is addressed on lines A0–A12, where A0 is the MSB and A12 is the LSB. Address lines A0–A4 are also used in the programming of the auxiliary memory functions to address the internal configuration and write protection registers.

the data bus (pins D0 . . . D7, & pin D8/PE<sub>⌋</sub>)

The SRAM data bus is composed of signals D0–D7 and D8/PE<sub>⌋</sub>. Signal D8/PE<sub>⌋</sub> can represent either a ninth data bit or a parity error. In addition, D8/PE<sub>⌋</sub> has a special output buffer which can be set up as either a 3-state or open-collector device (for use in systems having wire-anded parity reporting schemes).

CONTROL SIGNALS					MACHINE CYCLE
CS <sub>⌋</sub>	RST <sub>⌋</sub>	CT0	CT1	CT2	
X	L	L	X	X	Reset – Pipeline Mode: All buffers are disabled, parity and write protection turned off. Three rising edges of (CLK/WE <sub>⌋</sub> ) required to exit Reset state.
X	L	H	X	X	Reset – Conventional Mode: All buffers are disabled, parity and write protection turned off. Three rising edges of (CLK/WE <sub>⌋</sub> ) required to exit Reset state.
X	H	L	L	L	Halt Cycle: In pipelined mode, A0–A12, CS <sub>⌋</sub> , CT0–CT2 values are repeated from the previous clock cycle. In conventional mode, or after reset, HALT is treated as a deselect.
L	H	L	L	H	DMA Memory Write Cycle
L	H	X	H	L	Memory Read Cycle
L	H	L	H	H	CPU Memory Write Cycle
L	H	H	L	L	Auxiliary Function Control Register Read Cycle
L	H	H	L	H	Auxiliary Function Control Register Write Cycle
L	H	H	H	H	Memory Write: Override Write-protection
H	H	X	X	H	Deselect
H	H	X	H	X	Deselect
H	H	H	X	X	Deselect

TABLE 1 SRAM MACHINE CYCLE TYPES

### auxiliary memory functions

The auxiliary memory functions are selected by setting internal SRAM control registers. The configuration and write protection registers (collectively referred to as the auxiliary function control registers) have discrete internal addresses which can be accessed via the SRAM address bus. Address lines A0-A4 are used for this purpose. A function is selected by placing the auxiliary function control registers into specific logic states. Data bus line D0 passes the control bits to the registers and is also used in answering status requests. (The SRAM does not access data lines D1-D7 or D8/PE<sub>l</sub> during programming cycles.)

Since data line D0 and address lines A0-A4 are used for both programming and memory accessing, the SRAM must either be in a READ or WRITE Auxiliary Control Register Machine Cycle to interpret these signals as function selection instructions.

Table 2 lists the addresses of all of the auxiliary function control registers along with the corresponding function. The associated memory functions appear in Table 3.

### auxiliary function programming

The generic procedure for accessing the auxiliary memory functions is:

- 1) Place the SRAM in either the Read or Write Auxiliary Control Register machine cycle.
- 2) Place the address of the appropriate function control register on address lines A0-A4.
- 3a) If in the write mode, place the appropriate logical 1 or 0 data value on data line D0.  
or
- 3b) If in the read mode, examine data line D0 for the state of the control register.
- 4) Repeat steps 2 and 3 to set (fetch) additional function control bits.
- 5) Exit from the auxiliary control register read/write cycle.

### pipelined operations

As Table 3 indicates, the SRAM can be operated in a variety of pipelined configurations. In all of these modes, address and control signals can be overlapped with memory accesses and control operations. When switched into the memory access flow, the pipeline registers latch in the address bus and control line (CT0-CT2 and CS<sub>l</sub>) values on each rising edge of signal CLK/WE<sub>l</sub>. In a similar manner, a falling edge on signal CLK/WE<sub>l</sub> will enable the data bus output buffers (as is appropriate for the memory cycle and functional configuration). When the "next-cycle" parity reporting functions are selected, a parity pipeline register is switched into the path of signal D8/PE<sub>l</sub>. Typical waveforms for the pipelined memory cycle are illustrated in Figure 1.

MSB			LSB		FUNCTION OF BIT (#)	MEM. ADD. PROTECTED A0 ... A12	BIT LOCATION
A	A	A	A	A			
0	1	2	3	4			
L	L	L	L	L	CPU PROTECT K0	0000-03FF	WRITE PROTECT
L	L	H	L	L	CPU PROTECT K1	0400-07FF	WRITE PROTECT
L	H	L	L	L	CPU PROTECT K2	0800-0BFF	WRITE PROTECT
L	H	H	L	L	CPU PROTECT K3	0C00-0FFF	WRITE PROTECT
H	L	L	L	L	CPU PROTECT K4	1000-13FF	WRITE PROTECT
H	L	H	L	L	CPU PROTECT K5	1400-17FF	WRITE PROTECT
H	H	L	L	L	CPU PROTECT K6	1800-1BFF	WRITE PROTECT
H	H	H	L	L	CPU PROTECT K7	1C00-1FFF	WRITE PROTECT
L	L	L	L	H	DMA PROTECT K0	0000-03FF	WRITE PROTECT
L	L	H	L	H	DMA PROTECT K1	0400-07FF	WRITE PROTECT
L	H	L	L	H	DMA PROTECT K2	0800-0BFF	WRITE PROTECT
L	H	H	L	H	DMA PROTECT K3	0C00-0FFF	WRITE PROTECT
H	L	L	L	H	DMA PROTECT K4	1000-13FF	WRITE PROTECT
H	L	H	L	H	DMA PROTECT K5	1400-17FF	WRITE PROTECT
H	H	L	L	H	DMA PROTECT K6	1800-1BFF	WRITE PROTECT
H	H	H	L	H	DMA PROTECT K7	1C00-1FFF	WRITE PROTECT
L	L	L	H	L	PIPELINE ENABLE		CONF. G. REGISTER
H	L	L	H	L	PARITY BIT 1		CONF. G. REGISTER
L	H	L	H	L	PARITY BIT 2		CONF. G. REGISTER
H	H	X	H	L	RESERVED - NOT USABLE		
X	X	H	H	L	RESERVED - NOT USABLE		
X	X	X	H	H	RESERVED - NOT USABLE		

#1 - ACTIVE HIGH FUNCTION

TABLE 2 ADDRESSES OF THE AUXILIARY FUNCTION CONTROL REGISTERS

PIPE	PAR1	PAR2	PARITY	DR. PE	PIPELINED
L	L	L	None	Three-state	NO
L	L	H	Same cycle	Three-state	NO
L	H	L	Same cycle	Open-drain	NO
L	H	H	Same cycle	Three-state	NO
H	L	L	None	Three-state	YES
H	L	H	Same cycle	Three-state	YES
H	H	L	Next cycle	Open-drain	YES
H	H	H	Next cycle	Three-state	YES

TABLE 3 DECODED FUNCTIONS FOR THE PIPE-PAR1-PAR2 REGISTER GROUP

### parity operations

The SLC2189 has parity operations for both conventional and pipelined memory systems (see Table 3). The SRAM flags parity errors by sending a logical 0 over signal D8/PE<sub>0</sub>.

Since the parity checking operation cannot begin until the data is accessed and stabilizes, system throughput can be seriously affected. For this reason, a parity pipeline register can be switched into the D8/PE<sub>0</sub> signal path to allow error reporting on the subsequent machine cycle ("next-cycle" parity).

### the D8/PE<sub>0</sub> programmable output buffer

The SLC2189 is designed for use in memory systems of any word width. When needed, (as in systems with word widths exceeding 8-bits), the SRAM can be programmed to configure the D8/PE<sub>0</sub> output buffer as an open-drain device during parity operations. The open-drain configuration allows the parity signals from multiple SRAMs to be tied to a single data line and resolves the potential conflict of two or more devices being enabled simultaneously. When this feature is not selected, the output buffer performs like a normal 3-state device.

### write-protection

The write-protection architecture of the SRAM divides the memory space into eight blocks of 1,024 (1K) words. As Table 2 illustrates, two independent write-protection operations can be performed on each memory block. This scheme facilitates the development of memory systems which must be shared by multiple controllers — such as the popular CPU and DMA configuration — as the controllers can independently reserve their own memory blocks in a shared storage space.

The write-protection operations are initiated during auxiliary function control register WRITE cycles. The address of the auxiliary memory control register for an operation is loaded on the SRAM address bus (see Table 2) and a program bit is placed on data line D0. When a control register is set to one, its memory block becomes write-protected. If a write pulse is blocked, the PV<sub>0</sub> output is driven low to indicate the attempted violation.

As shown in Table 1, this device also features a special write-protection override mode which allows high priority system tasks (i.e. memory paging, priority management, error recovery) to gain access to these reserved locations, and free them up for further use.

### protection violation (PV<sub>0</sub>)

If a memory controller attempts to write to a protected block, the write operation will be disallowed and the protection violation will be reported as a logical zero on output signal PV<sub>0</sub>. During an auxiliary function READ/WRITE cycle, however, the SRAM drives PV<sub>0</sub> active to acknowledge that an auxiliary function machine cycle is occurring. In a pipeline mode, a falling edge on CLK/WE<sub>0</sub> will enable the PV<sub>0</sub> output buffer. In a conventional operating mode, PV<sub>0</sub> will only stabilize after input signals do so.



## machine cycle details

### the system clock (CLK/WE<sub>l</sub>)

The SLC2189 SRAM operates synchronously with respect to the system (or memory) clock. The clock is applied to signal pin CLK/WE<sub>l</sub>.

In the pipelined mode, the rising edge of the system clock is used to load machine cycle control signals CS<sub>l</sub>, CT0-CT2, and the contents of the address bus into the pipeline registers. The same clock transition also controls the writing of data into the memory array and the programming of the auxiliary function control registers. The falling edge of the system clock enables the output buffers, and D8/PE<sub>l</sub> and PV<sub>l</sub> when appropriate.

Figures 1 through 4 illustrate the relationships between the various machine cycles and the system clock.

### bus collision avoidance technique (BCAT)

In the pipeline mode the SRAM has a 3-state enable feature that virtually eliminates output signal contention with other IC's. Unless the SRAM is in a Halt cycle, outputs are all 3-stated when CLK/WE<sub>l</sub> is high. Outputs are enabled only when CLK/WE<sub>l</sub> is low. During a Halt Cycle, outputs are allowed to be enabled when CLK/WE<sub>l</sub> is high.

#### BCAT OUTPUT-STATE SUMMARY

CONTROL SIGNALS	CLK	SRAM OUTPUTS
Non-Halt	0	Can Enable
Non-Halt	1	All 3-State
Halt	0	Can Enable
Halt	1	Can Enable

### halt cycle

The halt cycle is primarily used in system debugging and in fault tolerant computing applications. In the pipeline mode, a "halt" causes the SRAM to repeat the previous machine cycle until a non-halt type instruction is placed on SRAM machine cycle control lines (CT0-CT2). System designers are cautioned to be aware of the fact that if the SRAM was in a write cycle prior to receiving the halt instruction, anything appearing on the data bus prior to the cancellation of the halt will be written to memory. If the previous cycle was a read cycle, normal BCAT operation is suspended and the outputs remain active while CLK/WE<sub>l</sub> is high.

If a halt instruction is received by the SRAM while it is in the conventional mode, the device is selected.

### reset (RST<sub>l</sub>)

The SRAM goes into a reset mode when the RST<sub>l</sub> signal goes low. Normal operations end, and all output buffers are asynchronously disabled. The 'reset' sets an internal counter which prevents escape until three rising edges are detected on CLK/WE<sub>l</sub> after RST<sub>l</sub> goes high. Control registers are set as shown in Table 4. The RST<sub>l</sub> line overrides all other inputs. RST<sub>l</sub> is the only asynchronous signal in both pipelined and conventional modes.

BIT	STATE AFTER RESET	FUNCTION
CPUWP0-7	0 (not protected)	CPU protection bits
DMAWP0-7	0 (not protected)	DMA protection bits
PIPE	$\overline{\text{CT0}}$	Pipeline control
PAR0	0 (No Parity)	Parity Control 0
PAR1	0 (No Parity)	Parity Control 1

TABLE 4 RESET STATES FOR THE AUXILIARY CONTROL REGISTERS

### pipeline/conventional selection at reset

When the RST<sub>l</sub> signal goes high, the value on machine cycle control line CT0 is examined so that the SRAM can "wake up" in either a conventional or pipelined mode. If a logical zero is detected, the SRAM will start up in the pipeline mode. If a logical one is detected, the SRAM will start up in the conventional mode. Table 5 contains the set-up and hold requirements necessary so that signal CT0 triggers this restart operation.

PARAMETER		MIN	TYP	MAX	UNIT
t <sub>rs</sub>	CT0 Setup before rising edge of RST <sub>l</sub>		9		ns
t <sub>rh</sub>	CT0 Hold after rising edge of RST <sub>l</sub>	-	0		ns

TABLE 5 RESET TIMING VALUES

### chip select (CS<sub>l</sub>)

The SRAM is 'selected' as long as a logical zero is applied to signal path CS<sub>l</sub>. In the pipelined mode, CS<sub>l</sub> is only sampled on the rising edge of CLK/WE<sub>l</sub>. Once sampled, it may change state without affecting the remainder of the selected operation. In the case of pipelined "next-cycle" parity operations, if CS<sub>l</sub> is low at the beginning of a read cycle, the parity error signal will be generated during the "next-cycle", regardless of any subsequent changes on CS<sub>l</sub>. Thus, the operation completes its normal duty cycle.

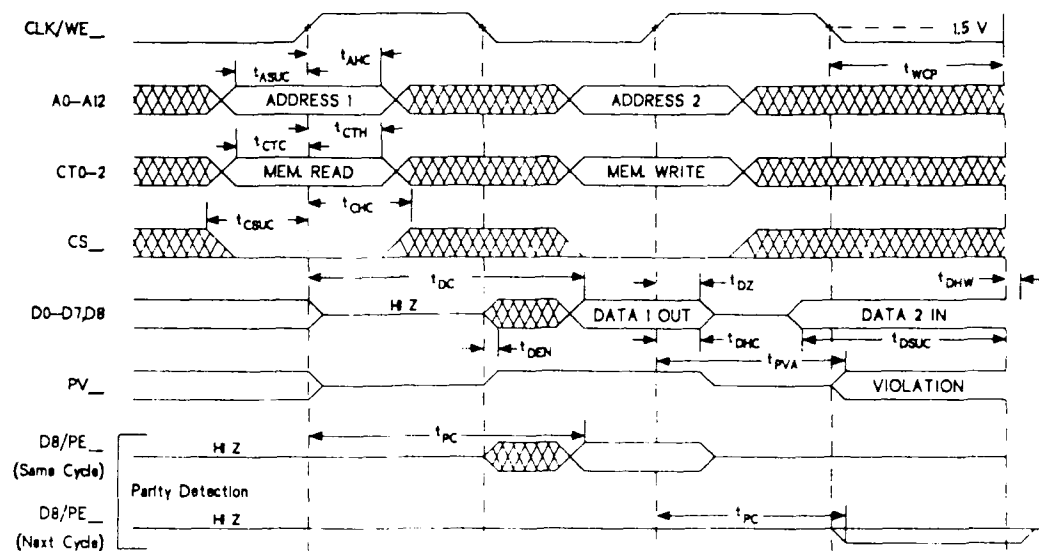


Figure 1 PIPELINED MEMORY CYCLE WAVEFORMS

PARAMETER	MIN	TYP	MAX	UNIT
$t_{ASUC}$		7		ns
$t_{AHC}$	-	0		ns
$t_{CSUC}$		5		ns
$t_{CHC}$	-	0		ns
$t_{DC}$		40		ns
$t_{DHC}$		4		ns
$t_{DSUC}$		13		ns
$t_{DHW}$	-	0		ns
$t_{DZ}$		5		ns
$t_{DEN}$		20		ns
$t_{WPC}$		22		ns
$t_{PC}$		50		ns
$t_{PVA}$		23		ns
$t_{CTC}$		5		ns
$t_{CTCH}$		14		ns
$t_{CTH}$	-	0		ns

§ Typical values are at  $V_{CC1} = 5\text{ V}$ ,  $V_{CC2} = 3.3\text{ V}$ ,  $GND = 0\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

TABLE 6 MEMORY CYCLE TIMING REQUIREMENTS - PIPELINED MODE

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PARAMETER	FROM	TO	NOTE	MIN	TYP	MAX	UNIT
$t_p$	CLK1	Valid Data on D0-D8/PE <sub>__</sub>	1, 3		40		ns
	CLK1	H-Z on D0-D8/PE <sub>__</sub>	1		5		
	CLK1	D8/PE <sub>__</sub>	1, 3		40		
	CLK1	D8/PE <sub>__</sub>	1, 4		50		
	CLK1	PV <sub>__</sub>			23		
	CLK1	D0-D8/PE <sub>__</sub>	2		20		ns

- Notes: 1. The duration of the High Clock state must be less than  $t_p$ .  
2. The logic levels on the data lines must be constant while the output buffers are enabled.  
3. When D8/PE<sub>\_\_</sub> is used as a data bit.  
4. When D8/PE<sub>\_\_</sub> is used as a same cycle parity bit.

TABLE 7 SRAM SWITCHING CHARACTERISTICS - PIPELINED MODE

PARAMETER	FROM	TO	MIN	TYP	MAX	UNIT
$t_{su}$	A0-A12	CLK1		7		ns
	CS <sub>__</sub>	CLK1		5		
	D0-D8/PE <sub>__</sub>	CLK1		13		
	CT0-CT2	CLK1		14		
$t_h$	CLK1	A0-A12		0		ns
	CLK1	CS <sub>__</sub>		0		
	CLK1	D0-D8/PE <sub>__</sub>		0		
	CLK1	CT0-CT2		0		

TABLE 8 SRAM SETUP REQUIREMENTS - PIPELINED MODE

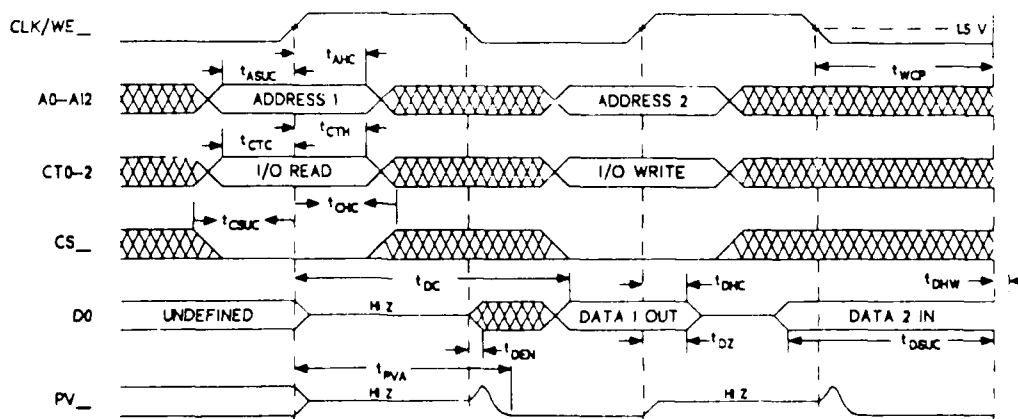


Figure 2 CONTROL REGISTER PROGRAMMING WAVEFORMS

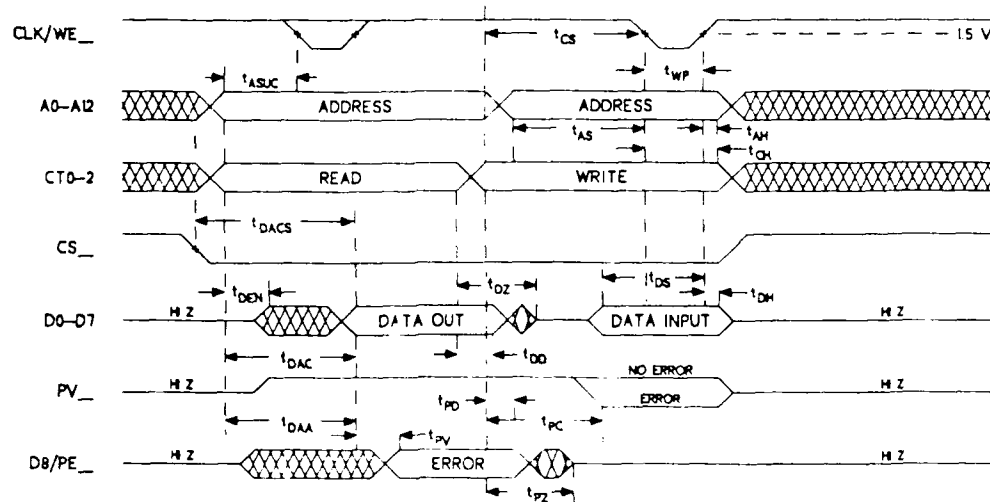


Figure 3 CONVENTIONAL MEMORY CYCLE WAVEFORMS

PARAMETER	MIN	TYP§	MAX	UNIT
t <sub>DAC</sub>		27		ns
t <sub>DAA</sub>		45		ns
t <sub>DD</sub>		9		ns
t <sub>DH</sub>	-	0		ns
t <sub>DS</sub>		13		ns
t <sub>WP</sub>		14		ns
t <sub>PA</sub>		-		ns
t <sub>PC</sub>		-		ns
t <sub>PV</sub>		-		ns
t <sub>PD</sub>		-		ns
t <sub>AS</sub>		-		ns
t <sub>AH</sub>	-	0		ns
t <sub>CS</sub>		-		ns
t <sub>CH</sub>	-	0		ns
t <sub>DEN</sub>		22		ns
t <sub>DZ</sub>		18		ns
t <sub>PZ</sub>		18		ns
t <sub>DACS</sub>		43		ns

§ Typical values are at VCC1 = 5 V, VCC2 = 3.3 V, GND = 0 V and T<sub>A</sub> = 25°C.

TABLE 9 MEMORY CYCLE TIMING REQUIREMENTS - CONVENTIONAL MODE

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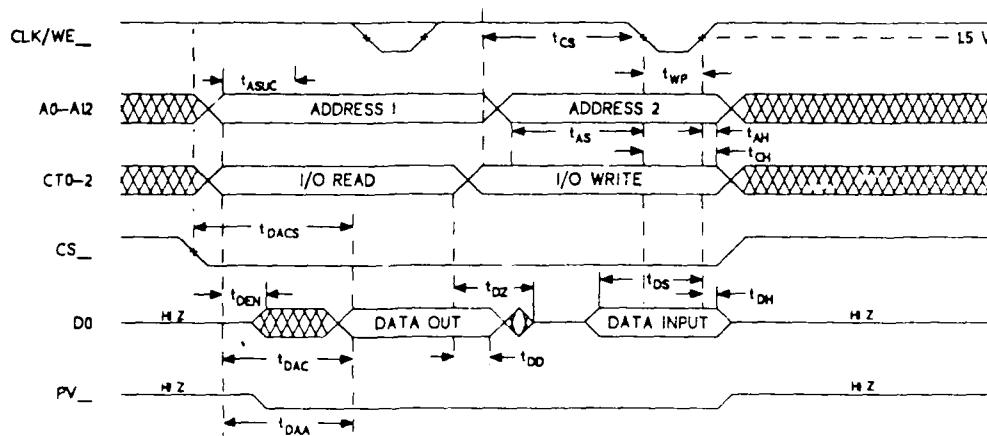


Figure 4 CONVENTIONAL CONTROL REGISTER PROGRAMMING WAVEFORMS

absolute maximum ratings over operating free-air temperature

Supply voltage $V_{CC1}$	5.5 V
Supply voltage $V_{CC2}$	3.6 V
Power dissipation (active)	— mW
(stand by)	— mW
Operating case temperature range, $T_C$	-55°C to 125°C
Storage temperature range	-65°C to 150°C

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recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V <sub>CC1</sub>	4.5	5.0	5.5	V
Supply voltage, V <sub>CC2</sub>	3.0	3.3	3.6	V
Supply voltage, GND		0.0		V
High-level input voltage, V <sub>IH</sub>	2.0		—	V
Low-level input voltage, V <sub>IL</sub>	—		0.8	V
Maximum cycle time, t <sub>C</sub>			—	ns
Operating free-air temperature, T <sub>A</sub>	—55			°C
Operating case temperature, T <sub>C</sub>			125	°C

electrical characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IH</sub> High-level input voltage		—	1.8		V
V <sub>IL</sub> Low-level input voltage			1.0	—	V
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = —18 mA			—	V
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V I <sub>OH</sub> = —4.0 mA	—	2.7		V
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V I <sub>OL</sub> = 8.0 mA		0.3	—	V
I <sub>OZH</sub> Off-state output current high-level voltage applied	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V V <sub>O</sub> = 2.4 V		—	—	µA
I <sub>OZL</sub> Off-state output current low-level voltage applied	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V V <sub>O</sub> = 0.5 V		—	—	µA
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V		1	—	µA
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		1	—	µA
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.0 V		—1	—	µA
I <sub>CC1</sub> Supply current	V <sub>CC</sub> = MAX	—	6	—	mA
I <sub>CC2</sub> Supply current	Active		140	—	mA
	Standby		15	—	mA

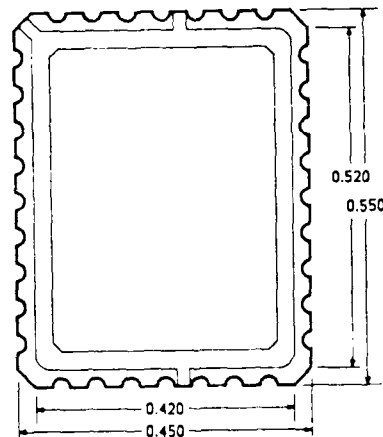
SLC2189  
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mechanical data

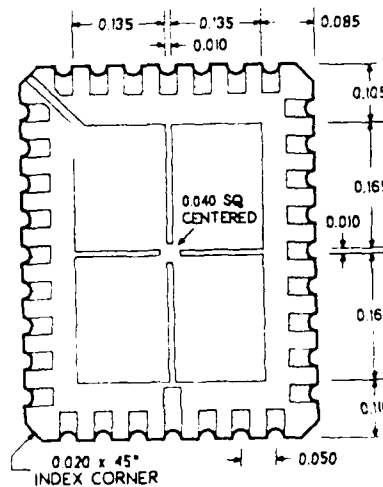
32 PAD LEADLESS CERAMIC CHIP CARRIER PACKAGE (LCC)

This hermetically sealed chip carrier package has a three-layer ceramic base with a metal lid and braze seal. This package is intended for surface mounting on solder pads on 0.050-inch centers.

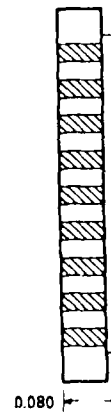


TOP VIEW

ALL DIMENSIONS  
IN INCHES



BOTTOM VIEW



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